STD 7000

7508

TTL Input/Output Card

USER'S MANUAL

A Pro-Log OPENWARE™ Product

FOREWORD

This manual explains how to use the Pro-Log 7508 TTL Input/Output Card. It is structured to reflect the answers to basic questions you might ask yourself about the 7508. We welcome your suggestions on how we can improve our instructions.

The 7508 is an OPENWARE product in the Pro-Log Series 7000 STD BUS hardware. Our products are modular and provide industrial managers with the means of using their own people to control the design, production, and maintenance of products that use STD BUS hardware. Pro-Log also offers courses on how to design with and use microprocessors and the STD BUS products.

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OPENWARE means Pro-Log products are designed to quality standards with readily available, second-sourced, industry standard components, clear and complete specifications, full documentation, and the option to purchase the manufacturing rights and drawings.

You may also find the following Pro-Log documents useful in your work: the Microprocessor User's Guide and the STD BUS Specification and Practice. If you would like a copy of these documents, please write to us on your company letterhead.

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REFERENCES/BIBLIOGRAPHY

STD BUS Specification and Practice. (Pro-Log Document #106989.)

Noise Reduction Techniques in Electronic Systems. John Wiley and Sons, New York.

Microprocessor User's Guide. (Pro-Log Document #101145.)

SPECIFICATIONS

PURPOSE

The 7508 is a 48-line TTL Input/Output Card that provides an interface between the industry standard 4-, 8-, 16-, and 24-I/O module mounting racks available from Opto-22, Gordos, IR Crydom, or equivalent manufacturers. The 7508 can directly control up to 48 AC or DC input or output modules in any combination or position.

These I/O modules are used to interface to motors, solenoids, heaters, transformers, lamps, and fans for industrial applications such as process control, machine tool control, and heating controls — as well as control of automatic test equipment.

Alternatively, the 7508 can be used as a general purpose I/O card or a short-distance (10 feet) parallel data communications card used for data transfers between PROM Programmers, printers, and other STD BUS systems.

FEATURES

- 48 individually addressable and fully buffered TTL I/O channels
- Easy connection for up to two 24-module I/O mounting racks
- Directly controls up to 48 AC or DC input or output modules
- Responds to an 8- or 10-bit I/O address
- Two latching header connectors
- Two +4.70 VDC at 500 mA power sources to power two I/O module mounting racks
- Low-pass input filters to reduce noise from industrial environments
- Single +5V operation
- Suitable for 8088, Z80, 8085, 6809, 6800, or other processors
- Two-year warranty

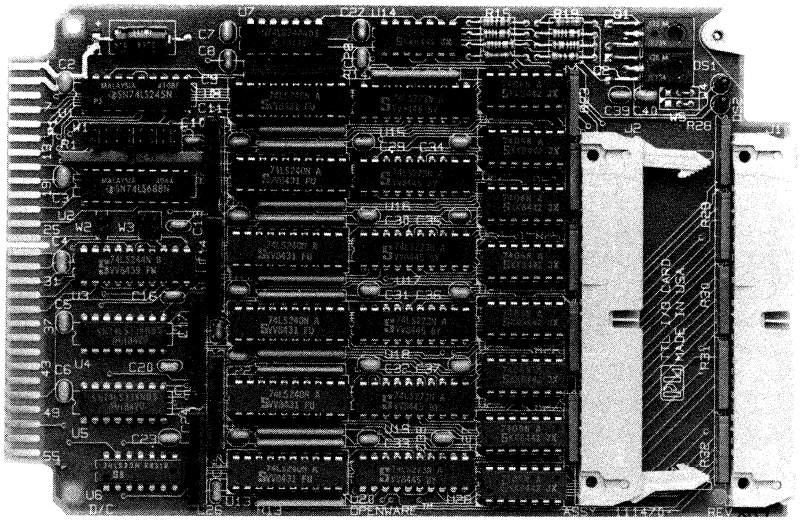


Figure 1-1. 7508 TTL Input/Output Card

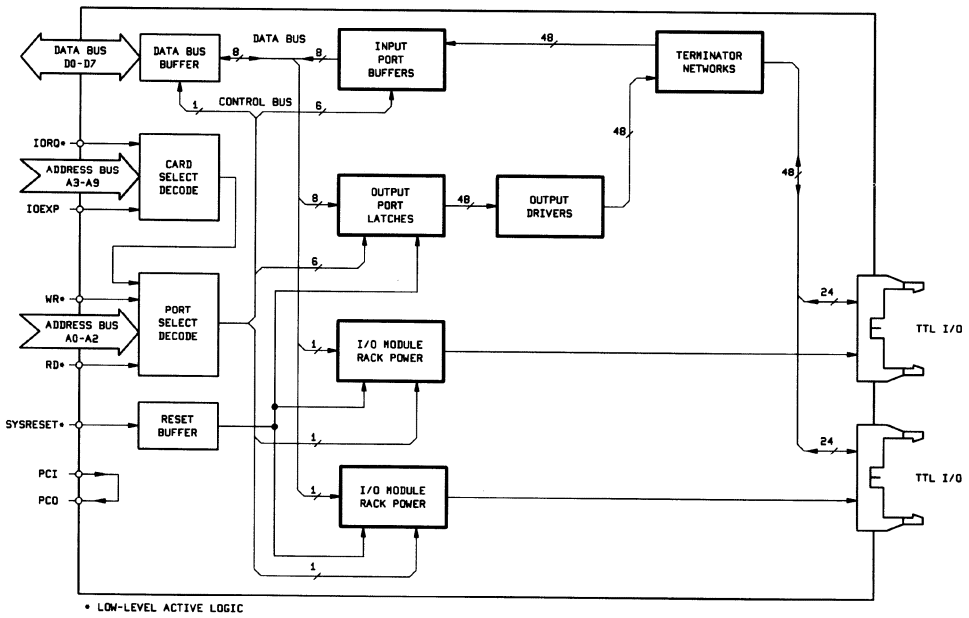


Figure 1-2. 7508 Block Diagram

FUNCTIONAL DESCRIPTION

DATA BUS BUFFER. This is an octal bus transceiver that provides buffering and direction control of the data bus. The data bus buffer prevents loading of the STD data bus when the 7508 card is not addressed.

CARD AND PORT SELECT DECODER. The input and output ports on the 7508 card respond to a jumper-selected combination of address lines, I/O Request (IORQ*), I/O Expansion (IOEXP), and either Read (RD*) or Write (WR*). As shipped, the 7508 decodes address lines A0 through A7, and is enabled with IOEXP low, allowing 256 port addresses (32 cards).

The 7508 can be configured to decode address lines A0 through A9. This feature is useful, but not essential, when operating with 16-bit processors that utilize 16-bit port addressing (e.g., the 8088 microprocessor used in the IBM Personal Computer). Ten-bit port addressing yields nonredundant decoding of 1024 I/O ports (128 7508 cards).

The 7508 can be enabled with IOEXP high, enabling an alternate 256 port (8-bit) or 1024 port (10-bit) addresses, or jumpered to ignore IOEXP.

The 7508 card occupies eight consecutive I/O addresses and is shipped with the ports mapped at 50 through 57 hex.

INPUT PORT BUFFERS. These buffers provide an interface between the signals and the user interface connectors and the STD BUS data bus. Only one of the six possible input buffers can be selected at a time, ensuring only eight of the 48 possible signal lines are transferred to the data bus during a card read.

OUTPUT PORT LATCHES. The Output Port Latches hold data present at last write signal and provide buffering from the data bus. A system reset clears all output port latches.

OUTPUT DRIVERS. These drivers provide sufficient drive capability and noise immunity of the signals available at user connectors.

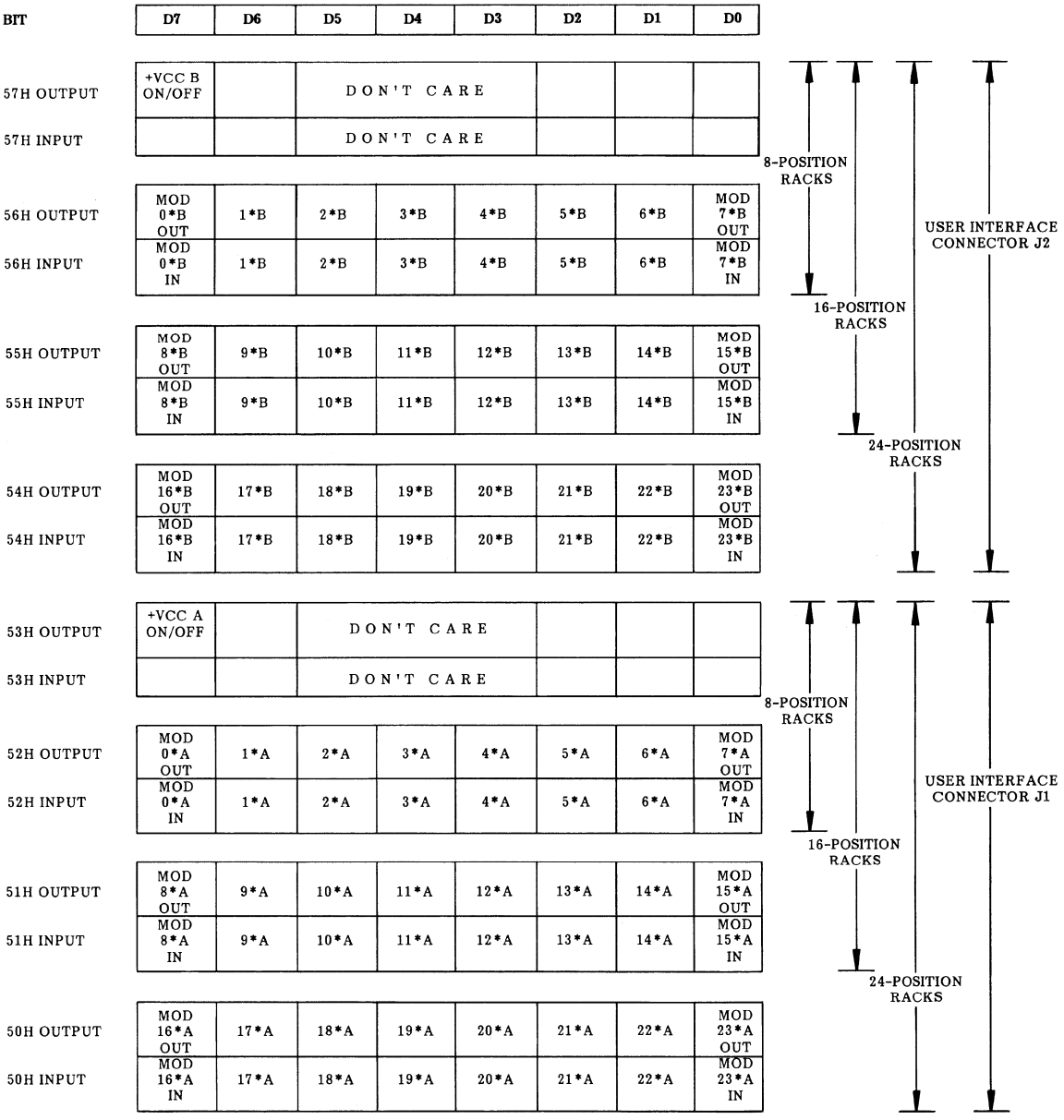


Figure 1-3. I/O Port Bit Assignment (As Shipped)

TERMINATOR NETWORKS. The terminator networks provide termination of signals on cables attached to user connectors. The networks are employed to minimize transients on each signal line.

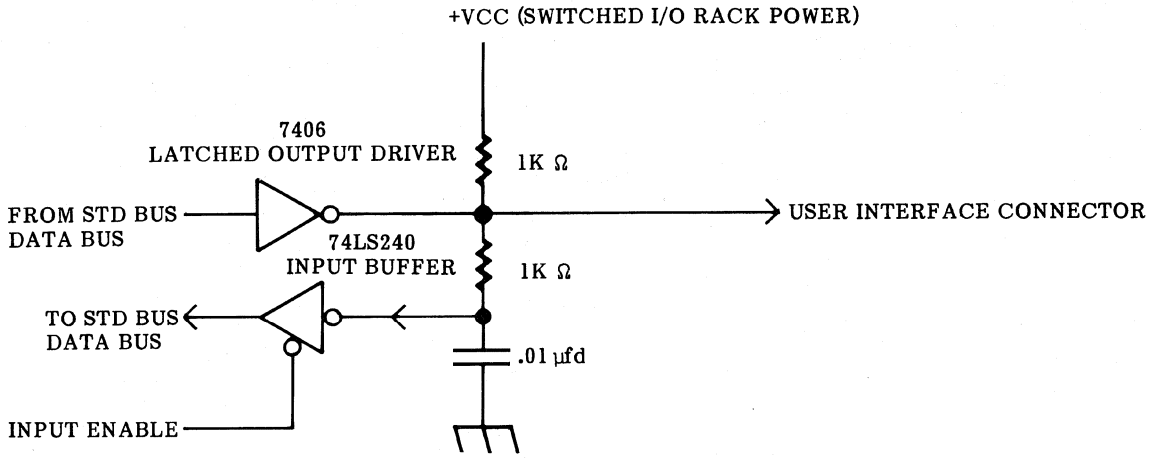


Figure 1-4. Typical I/O Line Termination

I/O MODULE RACK POWER

Each user interface connector is supplied with 4.70 VDC (typical) upon power-up or system reset. Under software control, Module Rack Power can be switched on and off.

The Module Rack Power jumper can be relocated so that power is applied to pin 49 of the user interface connector when the STD BUS system Vcc (+5 VDC typical) is on. The state of the Module Rack Power sources are indicated by LEDs.

USER INTERFACE CONNECTORS

There are two 50-pin latching connectors on the 7508 card. Each connector provides three 8-bit TTL buffered input ports, three 8-bit TTL latched output ports, and a +4.70 VDC (typical) source.

The 7508 card uses the industry-standard I/O module bus to communicate with the I/O module mounting rack(s). The bus consists of 24 bidirectional data lines alternated with 24 ground lines, a switched power line, and a ground power line. The 7508 I/O lines are typically routed over 50-conductor flat ribbon cable up to ten feet (3.05 meters). The pinout of the interface connectors on the 7508 card directly matches the pinout of the I/O rack.

As shipped, user interface connector J1 on the 7508 card is software compatible with the Pro-Log 7507 General Purpose Interface Card in pins, signals, and I/O port addressing. Note, however, that the user interface connector on the 7507 is a 50-pin edge connection.

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)					OUTPUT (LSTTL DRIVE)		
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
GND		OUT	2	1	50	13	MOD 23*A
			4	3	50	13	MOD 22*A
			6	5	50	13	MOD 21*A
			8	7	50	13	MOD 20*A
			10	9	50	13	MOD 19*A
			12	11	50	13	MOD 18*A
			14	13	50	13	MOD 17*A
			16	15	50	13	MOD 16*A
			18	17	50	13	MOD 15*A
			20	19	50	13	MOD 14*A
			22	21	50	13	MOD 13*A
			24	23	50	13	MOD 12*A
			26	25	50	13	MOD 11*A
			28	27	50	13	MOD 10*A
			30	29	50	13	MOD 9*A
			32	31	50	13	MOD 8*A
			34	33	50	13	MOD 7*A
			36	35	50	13	MOD 6*A
			38	37	50	13	MOD 5*A
			40	39	50	13	MOD 4*A
			42	41	50	13	MOD 3*A
			44	43	50	13	MOD 2*A
			46	45	50	13	MOD 1*A
			48	47	50	13	MOD 0*A
GND		OUT	50	49	500mA		*VCC A

*Low-level active logic
One LSTTL load = -0.4 mA

Figure 1-5. User Interface Connector J1

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)					OUTPUT (LSTTL DRIVE)		
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
GND		OUT	2	1	50	13	MOD 23*B
			4	3	50	13	MOD 22*B
			6	5	50	13	MOD 21*B
			8	7	50	13	MOD 20*B
			10	9	50	13	MOD 19*B
			12	11	50	13	MOD 18*B
			14	13	50	13	MOD 17*B
			16	15	50	13	MOD 16*B
			18	17	50	13	MOD 15*B
			20	19	50	13	MOD 14*B
			22	21	50	13	MOD 13*B
			24	23	50	13	MOD 12*B
			26	25	50	13	MOD 11*B
			28	27	50	13	MOD 10*B
			30	29	50	13	MOD 9*B
			32	31	50	13	MOD 8*B
			34	33	50	13	MOD 7*B
			36	35	50	13	MOD 6*B
			38	37	50	13	MOD 5*B
			40	39	50	13	MOD 4*B
			42	41	50	13	MOD 3*B
			44	43	50	13	MOD 2*B
			46	45	50	13	MOD 1*B
			48	47	50	13	MOD 0*B
GND		OUT	50	49	500mA		+VCC B

*Low-level active logic
One LSTTL load = -0.4 mA

Figure 1-6. User Interface Connector J2

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings
(Unless Otherwise Noted)

Supply Voltage, Vcc	0 to 7 V
Operating Free-Air Temperature	0°C to +65°C
Storage Temperature Range	-40°C to +75°C
Noncondensing Relative Humidity:	
Operating	5% to 95%
Nonoperating	5% to 95%

Operating Conditions

		MIN	TYP	MAX	UNIT
Vcc	Supply Voltage	4.75	5.00	5.25	V
	Operating Free-Air Temperature	0	+25	+65	°C
	Noncondensing Relative Humidity	5	—	95	%

Electrical Characteristics Over Free-Air Temperature Range
(Unless Otherwise Noted)

All logic signal levels related to the 7508 that appear on the bus conform to the STD BUS TTL requirements as specified in the General STD Series 7000 specification, document #111684.

7508 MTBF is 20 years (calculated using component standard failure rates specified in "Failure Rates & MTBF Calculation" document #111443).

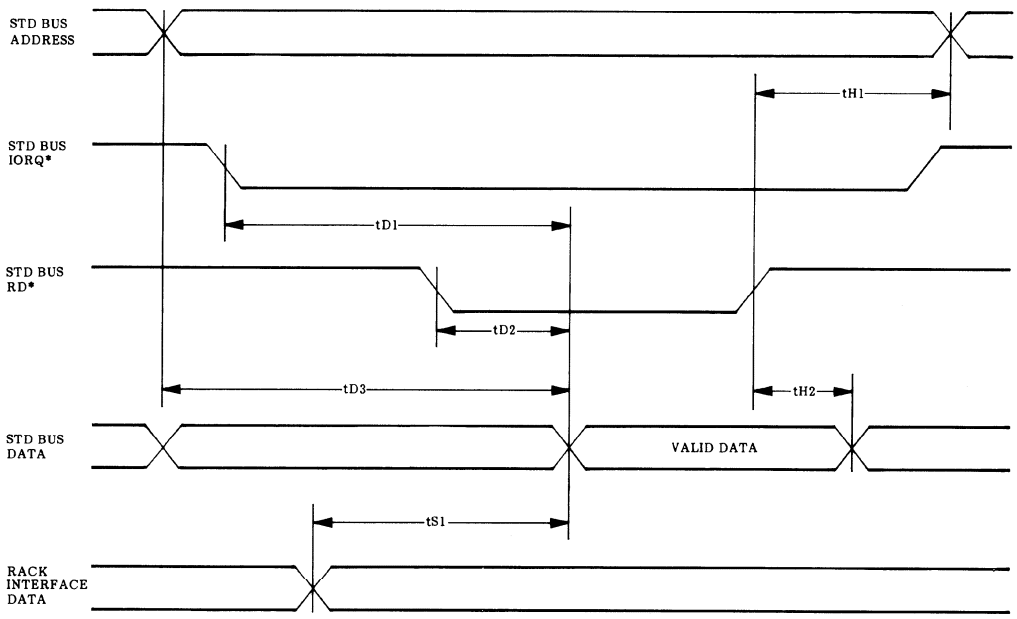
Parameter	Test Conditions	MIN	TYP	MAX	UNIT
Icc (Vcc Supply Current)	Includes 500 mA I/O module rack power at each user interface connector	—	1500	2000	mA

I/O Port Interface Characteristics
Over Operating Range

MNEM	PARAMETER	MIN	TYP	MAX	UNIT
V_{OL}	Low-level interface voltage (at 10 mA current level)	—	—	.80	Volt
I_{OL}	Low-level interface (at 0.70V level)	—	—	20.	mA
V_{OH}	High-level interface voltage	4.75	—	5.25	Volt
I_{OH}	High-level interface current (at 2.0V)	-3.0	—	—	mA
V_{+VCCA}	Supply voltage output to module rack	4.45	4.70	5.25	Volt
I_{VCCA}	Supply current output to module rack	—	—	500	mA
V_{VCCB}	Supply voltage output to module rack	4.45	4.70	5.25	Volt
I_{VCCB}	Supply current output to module rack	—	—	500	mA

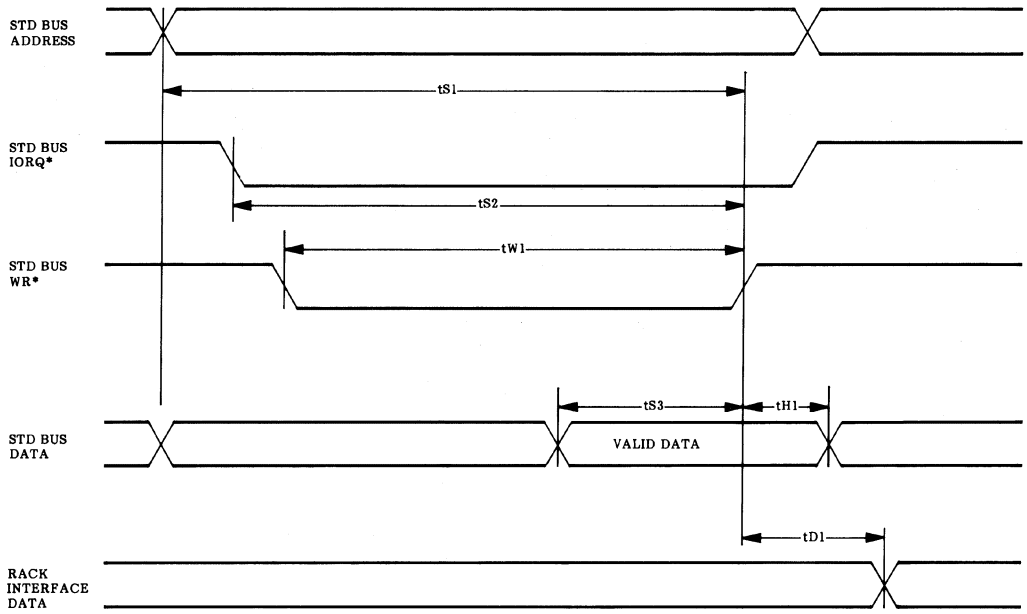
Switching Characteristics
Over Operating Range

MNEM	PARAMETER	FROM	TO	MIN	TYP	MAX	UNIT
T_{PLH}	Propagation Time	STD DATA BUS	USER IFC	-	-	60	ns
T_{PHL}	Propagation Time	STD DATA BUS	USER IFC	-	-	65	ns
T_{PLH}	Propagation Time	USER IFC	STD DATA BUS	3	5	8	ns
T_{PHL}	Propagation Time	USER IFC	STD DATA BUS	11	18	27	us



SYMBOL	PARAMETER	MIN	MAX	UNITS
tD1	Data delay from IORQ* active		135	ns
tD2	Data delay from RD* active		110	ns
tD3	Data delay from address valid		200	ns
tH1	Address hold after RD* inactive	10		ns
tH2	Data hold after RD* inactive	15		ns
tS1	Rack interface data setup before STD data valid		27	µs

Figure 1-7. Read Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
tD1	Rack interface data delay from WR* inactive		105	ns
tH1	Data hold after WR* inactive	55		ns
tS1	Address setup before WR* inactive	190		ns
tS2	IORQ* setup before WR* inactive	125		ns
tS3	Data setup before WR* inactive	25		ns
tW1	WR* pulse width	85		ns

Figure 1-8. Write Timing

CABLE FOR USE WITH THE 7508

The Pro-Log RC710 Interface Cable is an ideal interface between the 7508 and the industry-standard power I/O module mounting rack. The RC710 is a 6-foot, 50-pin flat ribbon cable with one end terminated with a strain-relieved, keyed mating connector for J1 or J2 on the 7508. The other end of the RC710 cable is terminated with a 50-pin I/O module mounting rack standard card edge connector. The 7508 provides adjacent grounds for each signal line. Two RC710 cables are necessary to fully utilize the 7508 card.

Mating Plugs for the User Interface Connectors (J1, J2)

MANUFACTURER	PART NUMBER
T&B/Ansley	609-5041
AMP	1-499933-0
SAE	CP6350BRPS
Winchester	81-50-112

MECHANICAL SPECIFICATION

The 7508 meets all general mechanical specifications of the STD BUS Series 7000 as given in the General STD Series 7000 Specification, document #111688. Overall card length (including connector latches) is 7.50 inches.

Card Spacing: Requires one .5-inch card slot.

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1**	55**	8	7	55**	1**	D3
D6	1**	55**	10	9	55**	1**	D2
D5	1**	55**	12	11	55**	1**	D1
D4	1**	55**	14	13	55**	1**	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Low-level active logic
** Only when the card is processor selected
One LSTTL load = -0.4 mA

Figure 1-9. STD Edge Connector

Reference Specifications

"General STD Series 7000 and 70C00 Specification" (document #111688)

"Failure Rates and MTBF Calculation" (document #111443)

Both the "General STD Series 7000 and 70C00 Specification" and the "Failure Rates and MTBF Calculation" documents can be found in the Pro-Log "STD BUS Technical Manual and Product Catalog" (Feb '85 edition).

INSTALLATION

> **CAUTION**
>
> To prevent possible damage to your STD BUS system make sure power is **off** before inserting a card into the card rack or removing a card from the card rack.

The 7508 TTL I/O card operates as part of an STD BUS card rack system. It plugs directly into the STD BUS backplane. The 7508 can be inserted into any slot in the card rack. It should be inserted with the card ejector tab at the top of the card, as shown in figure 2-1.

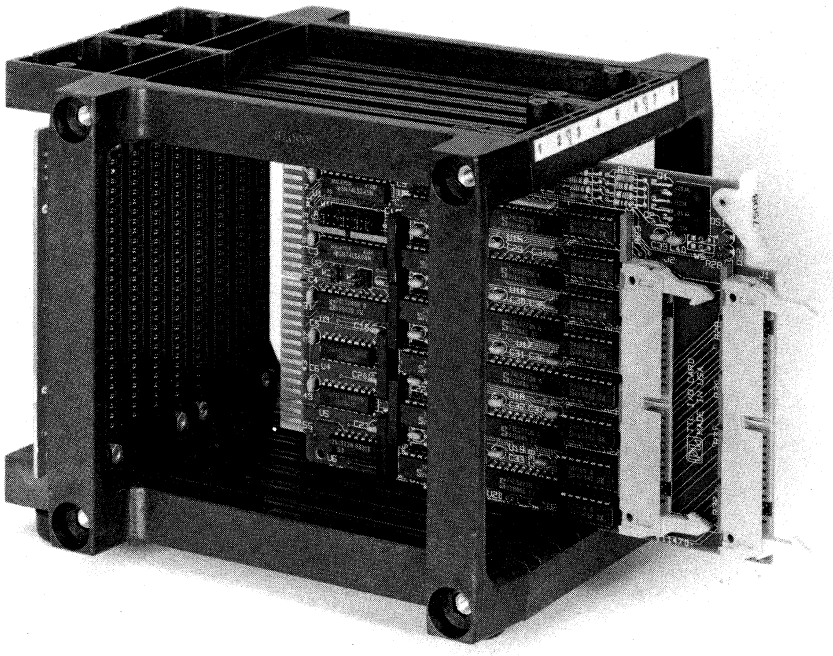


Figure 2-1. Installation

CARD LAYOUT AND JUMPERS

The 7508 has onboard jumpers to configure the card to meet system requirements. The jumper configurations consist of unshrouded headers and shorting connectors. The shorting connectors can be removed and installed without the use of soldering equipment. Figure 2-2 lists sources for the shorting connectors.

Figure 2-3 provides a reference for the location and a brief description of each jumper on the 7508.

SOURCE	PART NUMBER
Pro-Log	902520
Elco	008261024200870
Amp	531220-3

Figure 2-2. Sources for Shorting Connector

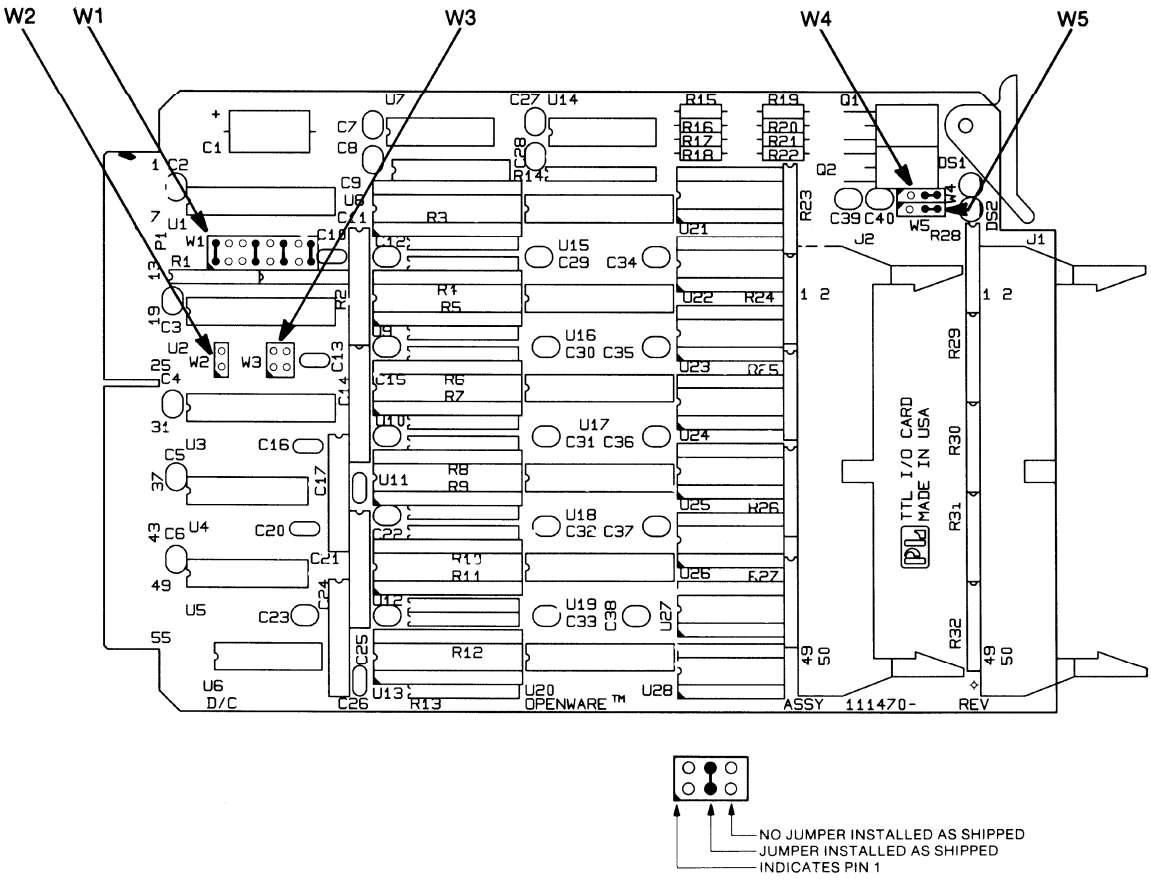


Figure 2-3. Physical Layout and Jumper Options

JUMPER GROUP	JUMPER INSTALLED	JUMPER REMOVED	DESCRIPTION	AS SHIPPED JUMPER
W1			**CARD SELECT DECODE**	
	1-2	—	• Enabled with IOEXP low (W2 removed)	*
	—	1-2	• Enabled with IOEXP high (W2 removed)	
	3-4 through 15-16		• Determine the I/O port address mapping (refer to I/O Mapped Card Addressing, page 2-4).	7-8 11-12 15-16
W2			**IOEXP DISABLE**	
	1-2	—	• Disregards IOEXP (W1 1-2 removed)	
	—	1-2	• Allows W1 1-2 to determine IOEXP enabling	*
W3			**ADDRESS DECODE**	
	1-2,3-4	—	• 10-bit port address decoding (A0-A9)	
	—	1-2,3-4	• 8-bit port address decoding (A0-A7)	*
W4			**MODULE RACK POWER +VCC B**	
	1-2	2-3	• +VCC applied to J2, pin 49	
	2-3	1-2	• Software controlled	*
W5			**MODULE RACK POWER +VCC A**	
	1-2	2-3	• +VCC applied to J1, pin 49	
	2-3	1-2	• Software controlled	*

Figure 2-3. (Continued)

I/O MAPPED CARD ADDRESSING

In normal operation, the 7508 is addressed directly by the processor card. The input and output ports respond to a jumper-selected combination of address lines, I/O Request (IORQ*), I/O Expansion (IOEXP), and either Read (RD*) or Write (WR*). As shipped, the 7508 decodes address lines A0 through A7.

The 7508 occupies eight consecutive I/O addresses regardless of its mapping assignment. The card is shipped with the eight ports mapped to hex addresses 50 to 57. You may retain these addresses or change them by moving the installed jumpers in the W1 header. While the card's port addresses are generally arbitrary, they must differ from all other I/O port addresses in the system. If they do not differ, multiple cards will respond to the same I/O read instruction, resulting in bus contention.

CHANGING THE PORT ADDRESS

The 7508 can be remapped anywhere within the 256-port addressing range of most processors. To change the I/O addressing, move the jumpers in the W1 header. Figure 2-3, page 2-2, shows the W1 header location and jumper installations as shipped. Figure 2-4, page 2-5, shows the jumper positions required for alternate mapping.

IOEXP

The I/O expansion line (IOEXP) of the STD BUS allows a system to access 512 I/O ports rather than the standard 256. As shipped, the 7508 is enabled with IOEXP in the low state. Pro-Log processor cards typically connect the IOEXP line to ground. The 7508 can be enabled with IOEXP high by removing jumper W1 1-2. To ignore IOEXP, remove the jumper at W1 1-2 and install a jumper at W2 1-2.

ADDRESS RANGE		CARD SELECT DECODE HEADER W1							
Interface Conn. J1	J2	(2) 1-2	(3) 3-4	(3) 5-6	7-8	9-10	11-12	13-14	15-16
00-03	04-07	x			x	x	x	x	x
08-0B	0C-0F	x			x	x	x	x	
10-13	14-17	x			x	x	x		x
18-1B	1C-1F	x			x	x	x		
20-23	24-27	x			x	x		x	x
28-2B	2C-2F	x			x	x		x	
30-33	34-37	x			x	x			x
38-3B	3C-3F	x			x	x			
40-43	44-47	x			x		x	x	x
48-4B	4C-4F	x			x		x	x	
50-53	54-57	x			x		x		x
58-5B	5C-5F	x			x		x		
60-63	64-67	x			x			x	x
68-6B	6C-6F	x			x			x	
70-73	74-77	x			x				x
78-7B	7C-7F	x			x				
80-83	84-87	x				x	x	x	x
88-8B	8C-8F	x				x	x	x	
90-93	94-97	x				x	x		
98-9B	9C-9F	x				x	x		
A0-A3	A4-A7	x				x		x	x
A8-AB	AC-AF	x				x		x	
B0-B3	B4-B7	x				x			x
B8-BB	BC-BF	x				x			
C0-C3	C4-C7	x					x	x	x
C8-CB	CC-CF	x					x	x	
D0-D3	D4-D7	x					x		x
D8-DB	DC-DF	x					x		
E0-E3	E4-E7	x						x	x
E8-EB	EC-EF	x						x	
F0-F3	F4-F7	x							x
F8-FB	FC-FF	x							

(1)

x Indicates jumper installed

(1) As shipped

(2) IOEXP jumper — remove for alternate 256 I/O port mapping

(3) Used with W3 for 10-bit address line decoding

Figure 2-4. Eight-Bit Port Address Mapping

TEN-BIT PORT ADDRESSING

The 8088 microprocessor (used in the IBM PC) provides a 16-bit I/O port address during each I/O operation. Using address lines A0-A15 yields a possible 64K I/O ports. In order to utilize the I/O addressing capability of the 8088 more fully, the 7508 card offers address lines A8 and A9 for decoding. Installing a jumper at W3 pins 1-2 (A9) and 3-4 (A8) will allow nonredundant decoding of 128 7508 cards. Figure 2-5 shows the jumper positions for 10-bit port address mapping.

ADDRESS RANGE		CARD SELECT DECODE HEADER W1 (2)							
Interface Conn. J1	J2	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16
0000-0003	0004-0007		x	x	x	x	x	x	x
0008-000B	000C-000F		x	x	x	x	x	x	
0010-0013	0014-0017		x	x	x	x	x		x
0018-001B	001C-001F		x	x	x	x	x		
0020-0023	0024-0027		x	x	x	x		x	x
0028-002B	002C-002F		x	x	x	x		x	
0030-0033	0034-0037		x	x	x	x			x
0038-003B	003C-003F		x	x	x	x			
0040-0043	0044-0047		x	x	x		x	x	x
0048-004B	004C-004F		x	x	x		x	x	
0050-0053	0054-0057		x	x	x		x		x
0058-005B	005C-005F		x	x	x		x		
0060-0063	0064-0067		x	x	x			x	x
0068-006B	006C-006F		x	x	x			x	
0070-0073	0074-0077		x	x	x				x
0078-007B	007C-007F		x	x	x				
0080-0083	0084-0087		x	x		x	x	x	x
0088-008B	008C-008F		x	x		x	x	x	
0090-0093	0094-0097		x	x		x	x		x
0098-009B	009C-009F		x	x		x	x		
00A0-00A3	00A4-00A7		x	x		x		x	x
00A8-00AB	00AC-00AF		x	x		x		x	
00B0-00B3	00B4-00B7		x	x		x			x
00B8-00BB	00BC-00BF		x	x		x			
00C0-00C3	00C4-00C7		x	x			x	x	x
00C8-00CB	00CC-00CF		x	x			x	x	
00D0-00D3	00D4-00D7		x	x			x		x
00D8-00DB	00DC-00DF		x	x			x		
00E0-00E3	00E4-00E7		x	x				x	x
00E8-00EB	00EC-00EF		x	x				x	
00F0-00F3	00F4-00F7		x	x					x
00F8-00FB	00FC-00FF		x	x					

(1)

ADDRESS RANGE		CARD SELECT DECODE HEADER W1 (2)							
Interface Conn. J1	J2	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16
0100-0103	0104-0107		x		x	x	x	x	x
0108-010B	010C-010F		x		x	x	x	x	
0110-0113	0114-0117		x		x	x	x		x
0118-011B	011C-011F		x		x	x	x		
0120-0123	0124-0127		x		x	x		x	x
0128-012B	012C-012F		x		x	x		x	
0130-0133	0134-0137		x		x	x			x
0138-013B	013C-013F		x		x	x			
0140-0143	0144-0147		x		x		x	x	x
0148-014B	014C-014F		x		x		x	x	
0150-0153	0154-0157		x		x		x		x
0158-015B	015C-015F		x		x		x		
0160-0163	0164-0167		x		x			x	x
0168-016B	016C-016F		x		x			x	
0170-0173	0174-0177		x		x				x
0178-017B	017C-017F		x		x				
0180-0183	0184-0187		x			x	x	x	x
0188-018B	018C-018F		x			x	x	x	
0190-0193	0194-0197		x			x	x		x
0198-019B	019C-019F		x			x	x		
01A0-01A3	01A4-01A7		x			x		x	x
01A8-01AB	01AC-01AF		x			x		x	
01B0-01B3	01B4-01B7		x			x			x
01B8-01BB	01BC-01BF		x			x			
01C0-01C3	01C4-01C7		x				x	x	x
01C8-01CB	01CC-01CF		x				x	x	
01D0-01D3	01D4-01D7		x				x		x
01D8-01DB	01DC-01DF		x				x		
01E0-01E3	01E4-01E7		x					x	x
01E8-01EB	01EC-01EF		x					x	
01F0-01F3	01F4-01F7		x						x
01F8-01FB	01FC-01FF		x						

(1)

x Indicates jumper installed.

(1) Redundantly mapped for hex 1XXX-FXXX (W2 removed).
Redundantly mapped for hex X4XX, X8XX, or XCXX.

(2) W3 1-2, 3-4 installed.

Figure 2-5. Ten-Bit Port Address Mapping

ADDRESS RANGE		CARD SELECT DECODE HEADER W1 (2)							
Interface Conn. J1	J2	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16
0200-0203	0204-0207			x	x	x	x	x	x
0208-020B	020C-020F			x	x	x	x	x	
0210-0213	0214-0217			x	x	x	x		x
0218-021B	021C-021F			x	x	x	x		
0220-0223	0224-0227			x	x	x		x	x
0228-022B	022C-022F			x	x	x		x	
0230-0233	0234-0237			x	x	x			x
0238-023B	023C-023F			x	x	x			
0240-0243	0244-0247			x	x		x	x	x
0248-024B	024C-024F			x	x		x	x	
0250-0253	0254-0257			x	x		x		x
0258-025B	025C-025F			x	x		x		
0260-0263	0264-0267			x	x			x	x
0268-026B	026C-026F			x	x			x	
0270-0273	0274-0277			x	x				x
0278-027B	027C-027F			x	x				
0280-0283	0284-0287			x		x	x	x	x
0288-028B	028C-028F			x		x	x	x	
0290-0293	0294-0297			x		x	x		x
0298-029B	029C-029F			x		x	x		
02A0-02A3	02A4-02A7			x		x		x	x
02A8-02AB	02AC-02AF			x		x		x	
02B0-02B3	02B4-02B7			x		x			x
02B8-02BB	02BC-02BF			x		x			
02C0-02C3	02C4-02C7			x			x	x	x
02C8-02CB	02CC-02CF			x			x	x	
02D0-02D3	02D4-02D7			x			x		x
02D8-02DB	02DC-02DF			x			x		
02E0-02E3	02E4-02E7			x				x	x
02E8-02EB	02EC-02EF			x				x	
02F0-02F3	02F4-02F7			x					x
02F8-02FB	02FC-02FF			x					

(1)

ADDRESS RANGE		CARD SELECT DECODE HEADER W1 (2)							
Interface Conn. J1	J2	1-2	3-4	5-6	7-8	9-10	11-12	13-14	15-16
0300-0303	0304=0307				x	x	x	x	x
0308-030B	030C-030F				x	x	x	x	
0310-0313	0314-0317				x	x	x		x
0318-031B	031C-031F				x	x	x		
0320-0323	0324-0327				x	x		x	x
0328-032B	032C-032F				x	x		x	
0330-0333	0334-0337				x	x			x
0338-033B	033C-033F				x	x			
0340-0343	0344-0347				x		x	x	x
0348-034B	034C-034F				x		x	x	
0350-0353	0354-0357				x		x		x
0358-035B	035C-035F				x		x		
0360-0363	0364-0367				x			x	x
0368-036B	036C-036F				x			x	
0370-0373	0374-0377				x				x
0378-037B	037C-037F				x				
0380-0383	0384-0387					x	x	x	x
0388-038B	038C-038F					x	x	x	
0390-0393	0394-0397					x	x		x
0398-039B	039C-039F					x	x		
03A0-03A3	03A4-03A7					x		x	x
03A8-03AB	03AC-03AF					x		x	
03B0-03B3	03B4-03B7					x			x
03B8-03BB	03BC-03BF					x			
03C0-03C3	03C4-03C7						x	x	x
03C8-03CB	03CC-03CF						x	x	
03D0-03D3	03D4-03D7						x		x
03D8-03DB	03DC-03DF						x		
03E0-03E3	03E4-03E7							x	x
03E8-03EB	03EC-03EF							x	
03F0-03F3	03F4-03F7								x
03F8-03FB	03FC-03FF								

(1)

x Indicates jumper installed.

(1) Redundantly mapped for hex 1XXX-FXXX (W2 removed).
Redundantly mapped for hex X4XX, X8XX, or XCXX.

(2) W3 1-2, 3-4 installed.

Figure 2-5. (Continued)

I/O PORT BIT ASSIGNMENT

The bit assignment of each input and output port on the 7508 card is illustrated in figure 2-6. The port addresses shown reflect the configuration of the 7508 as shipped. The bits used when interfacing to an 8-, 16-, or 24-I/O module mounting rack are also indicated.

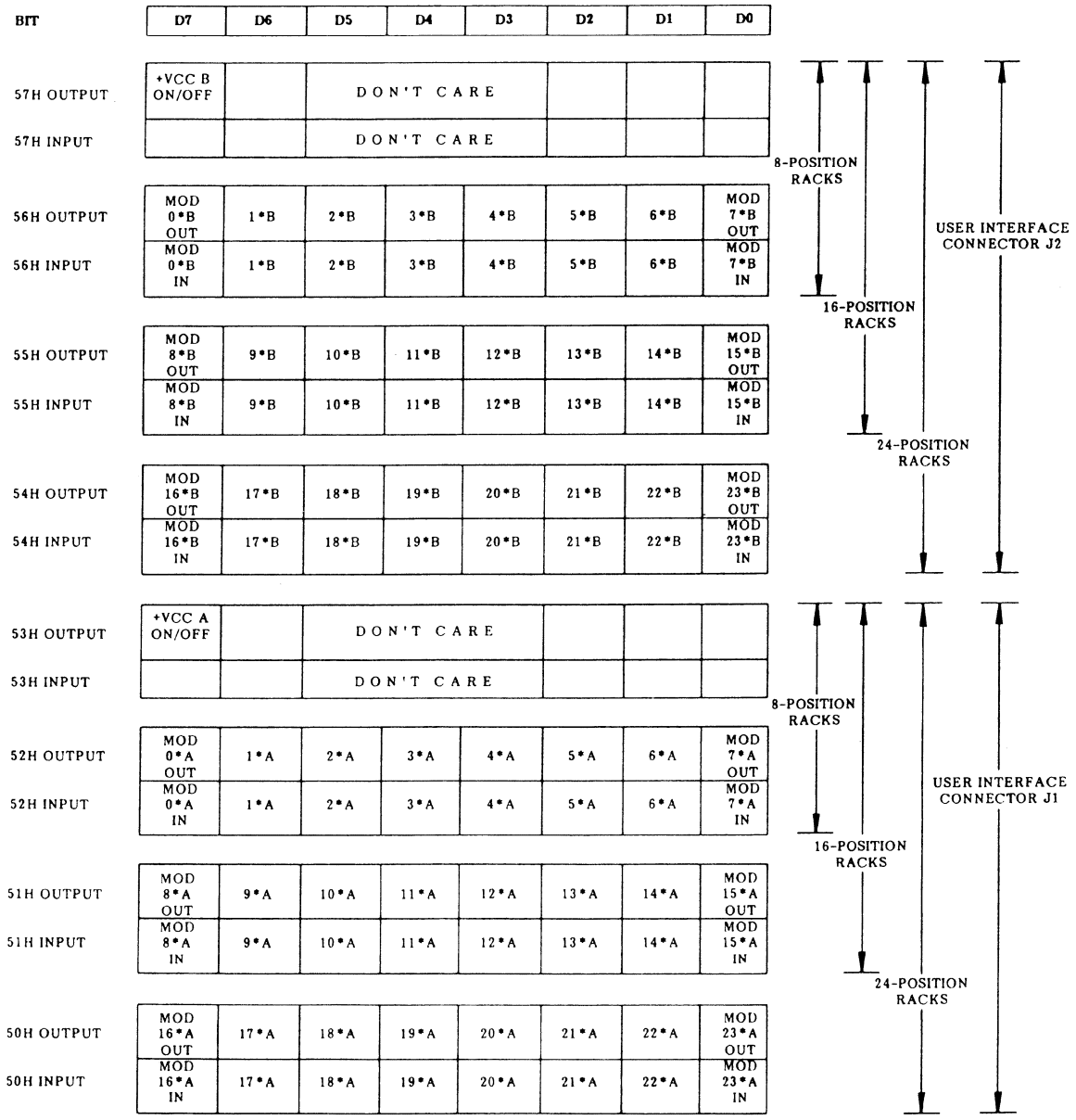


Figure 2-6. I/O Port Bit Assignment (As Shipped)

I/O PORT INTERFACE

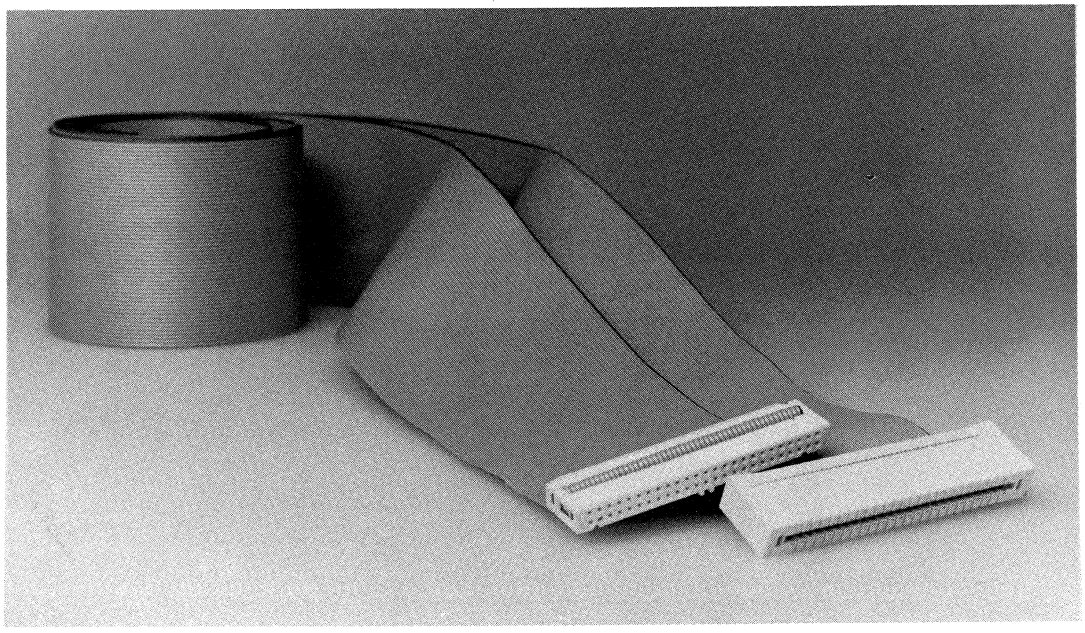
There are two 50-pin latching connectors on the 7508 card. The connectors are labeled J1 and J2 in figure 2-3, page 2-2. Each connector provides three 8-bit TTL buffered input ports, three 8-bit TTL latched output ports, and a +4.70 VDC (typical) source (see Specifications, page 2-11). The drive and load characteristics of the signals at J1 and J2 are shown in figures 2-10 and 2-11, pages 2-15 and 2-16.

As shipped, connector J1 on the 7508 card is software compatible with the Pro-Log 7507 General Purpose Interface Card in pins, signals, and I/O port addressing. Note, however, that the user interface connector on the 7507 is a 50-pin card edge connection.

The cabling between the 7508 and the peripheral will probably be exposed to some level of electromagnetic interference (EMI). This "noise" will usually be the main factor in limiting interface cable length. The highest operating frequency of any I/O line will also be limited by cable length due to cable reactance and settling time. When cable lengths beyond 10 feet are to be used, evaluate the cable and peripheral manufacturers' specifications and refer to the 7508 specifications in this manual (starting on page 2-11) to assure reliable operation. Refer also to References/Bibliography, page vi.

For custom wire cable assemblies, Pro-Log has tested and found the following mating connectors for J1 or J2 to be acceptable: T&B/Ansley 609-5041, AMP 1-499933-0, SAE CP6350BRPS, and Winchester 81-50-112.

The Pro-Log RC710 Interface Cable is an ideal interface between the 7508 and the industry standard power I/O module mounting rack. The RC710 is a 50-pin flat ribbon cable six feet long with one end terminated with a strain relieved, keyed mating connector for J1 or J2 on the 7508. The other end of the RC710 cable is terminated with a 50-pin I/O module mounting rack standard card edge connector. The 7508 provides adjacent grounds for each signal line. Two RC710 cables are necessary to fully utilize the 7508 card.



TERMINATOR NETWORKS

A transient is a temporary current or voltage excursion occurring in a circuit due to a sudden change of voltage or current. To minimize transients, a terminating network is connected to each I/O line of the 7508. Figure 2-7 illustrates a typical 7508 I/O line termination.

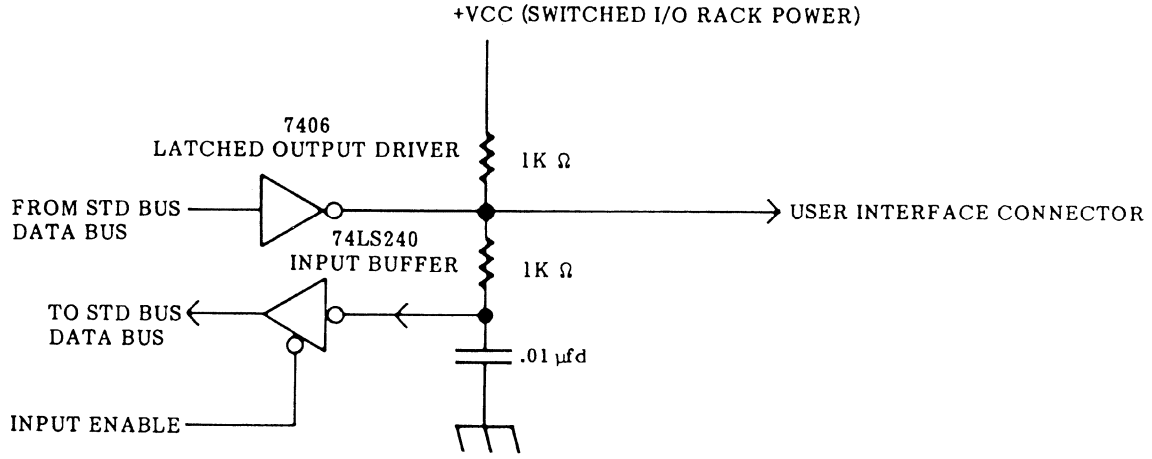


Figure 2-7. Typical I/O Line Termination

MODULE RACK POWER

As shipped, bit 7 of ports 53 and 57 hex is used to control the Module Rack Power line (pin 49) of J1 (+VCC A) and J2 (+VCC B) respectively. Each user interface connector is supplied with +4.70 VDC (typical) upon power-up or pushbutton reset. Under software control, bit 7 turns the Module Rack Power off or on. A one will turn power off; a zero will turn power on.

With Module Rack Power jumper W5 (W4) relocated to pins 1-2, power is applied to pin 49 of J1 (J2) when the STD BUS system VCC (+5 VDC typical) is on.

The state of the Module Rack Power sources are indicated by LEDs. DS1 illuminates when rack power is available at J1-49; DS2 illuminates when rack power is available at J2-49. The location of DS1 and DS2 is shown in figure 2-3, page 2-2.

CAUTION

There is no current limiting on these lines, so do not short them to ground. Connecting the cable backward may short the +VCC line to ground. Key the connector(s) to avoid this possibility.

SPECIFICATIONS

Electrical Requirements

		RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
MNEM.	**PARAMETER**	**MIN**	**TYP**	**MAX**	**MIN**	**MAX**	**UNITS**
V_{CC}	Supply Voltage	4.75	5.00	5.25	0	7.00	Volts

Electrical Specifications Over Operating Range

			OPERATING LIMITS		
MNEM.	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{CC}	V_{CC} Supply Current [1]	—	1500	2000	milliAmps
	STD BUS Input Load	See Pin List, figure 2-12			
	STD BUS Output Load	See Pin List, figure 2-12			

[1] Includes 500 milliAmps load at J1 (+VCC A) and J2 (+VCC B).

Environmental Specifications

		RECOMMENDED OPERATING LIMITS			ABSOLUTE NONOPERATING LIMITS		
MNEM.	**PARAMETER**	**MIN**	**TYP**	**MAX**	**MIN**	**MAX**	**UNITS**
--	Free Air Temperature	0	+25	+65	-40	+75	°C
--	Noncondensing Relative Humidity	5	—	95	5	95	%RH

I/O Port Interface Specification
Over Operating Free-Air Temperature Range

MNEM.	PARAMETER	OPERATING LIMITS			
		MIN	TYP	MAX	UNIT
V_{OL}	Low level interface voltage (at 10 mA current level)	--	--	.80	Volt
I_{OL}	Low level interface current (at 0.70V level)	—	—	20	mA
V_{OH}	High level interface voltage	4.75	—	5.25	Volt
I_{OH}	High level interface current (at 2.0V)	-3.0	—	—	mA
$V_{+VCC\ A}$	Supply voltage output to module rack	4.45	4.70	5.25	Volt
$I_{+VCC\ A}$	Supply current output to module rack	—	—	500	mA
$V_{+VCC\ B}$	Supply voltage output to module rack	4.45	4.70	5.25	Volt
$I_{+VCC\ B}$	Supply current output to module rack	—	—	500	mA

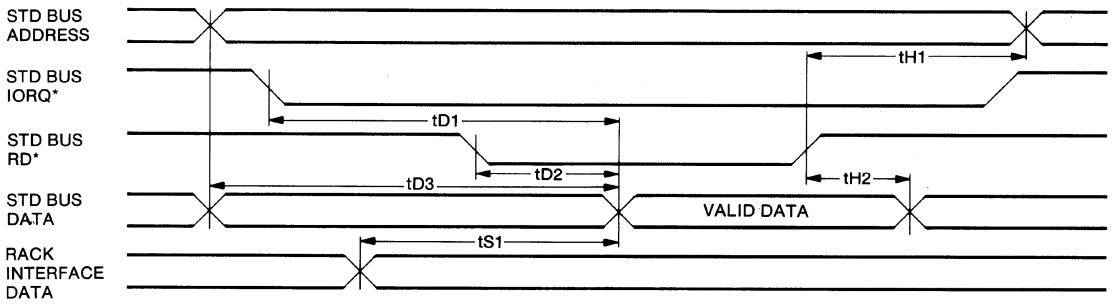
Switching Characteristics
Over Operating Free-Air Temperature Range

MNEM.	PARAMETER	FROM	TO	OPERATING LIMITS			
				MIN	TYP	MAX	UNIT
T_{PLH}	Propagation Time	STD DATA BUS	USER IFC	—	—	60	ns
T_{PHL}	Propagation Time	STD DATA BUS	USER IFC	—	—	65	ns
T_{PLH}	Propagation Time	USER IFC	STD DATA BUS	3	5	8	µs
T_{PHL}	Propagation Time	USER IFC	STD DATA BUS	11	18	27	µs

Mechanical Specifications

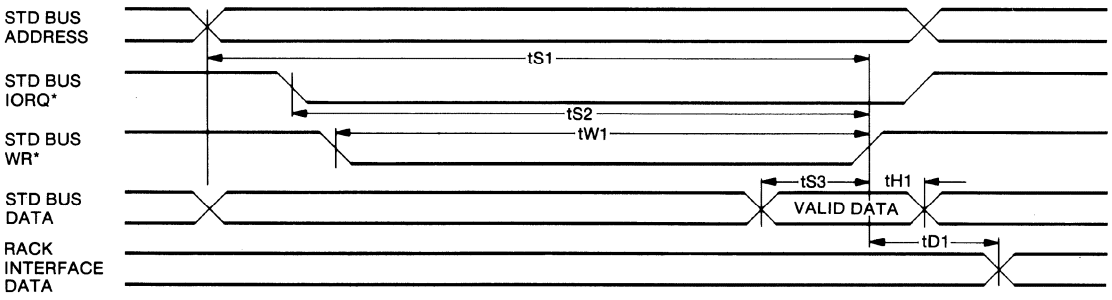
The 7508 meets all general mechanical specifications of the STD BUS.

Timing Specifications



SYMBOL	PARAMETER	MIN	MAX	UNITS
tD1	Data delay from IORQ* active		135	ns
tD2	Data delay from RD* active		110	ns
tD3	Data delay from address valid		200	ns
tH1	Address hold after RD* inactive	10		ns
tH2	Data hold after RD* inactive	15		ns
tS1	Rack interface data setup before STD data valid		27	µs

Figure 2-8. Read Timing



SYMBOL	PARAMETER	MIN	MAX	UNITS
tD1	Rack interface data delay from WR* inactive		105	ns
tH1	Data hold after WR* inactive	55		ns
tS1	Address setup before WR* inactive	190		ns
tS2	IORQ* setup before WR* inactive	125		ns
tS3	Data setup before WR* inactive	25		ns
tW1	WR* pulse width	85		ns

Figure 2-9. Write Timing

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC			PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
GND		OUT		2		1	50	13	MOD 23*A
				4		3	50	13	MOD 22*A
				6		5	50	13	MOD 21*A
				8		7	50	13	MOD 20*A
				10		9	50	13	MOD 19*A
				12		11	50	13	MOD 18*A
				14		13	50	13	MOD 17*A
				16		15	50	13	MOD 16*A
				18		17	50	13	MOD 15*A
				20		19	50	13	MOD 14*A
				22		21	50	13	MOD 13*A
				24		23	50	13	MOD 12*A
				26		25	50	13	MOD 11*A
				28		27	50	13	MOD 10*A
				30		29	50	13	MOD 9*A
				32		31	50	13	MOD 8*A
				34		33	50	13	MOD 7*A
				36		35	50	13	MOD 6*A
				38		37	50	13	MOD 5*A
				40		39	50	13	MOD 4*A
				42		41	50	13	MOD 3*A
				44		43	50	13	MOD 2*A
				46		45	50	13	MOD 1*A
				48		47	50	13	MOD 0*A
GND		OUT		50		49	500mA		*VCC A

*Low-level active logic

One LSTTL load = 0.4 mA

Figure 2-10. User Interface Connector J1

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)					OUTPUT (LSTTL DRIVE)		
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
GND		OUT	2	1	50	13	MOD 23*B
			4	3	50	13	MOD 22*B
			6	5	50	13	MOD 21*B
			8	7	50	13	MOD 20*B
			10	9	50	13	MOD 19*B
			12	11	50	13	MOD 18*B
			14	13	50	13	MOD 17*B
			16	15	50	13	MOD 16*B
			18	17	50	13	MOD 15*B
			20	19	50	13	MOD 14*B
			22	21	50	13	MOD 13*B
			24	23	50	13	MOD 12*B
			26	25	50	13	MOD 11*B
			28	27	50	13	MOD 10*B
			30	29	50	13	MOD 9*B
			32	31	50	13	MOD 8*B
			34	33	50	13	MOD 7*B
			36	35	50	13	MOD 6*B
			38	37	50	13	MOD 5*B
			40	39	50	13	MOD 4*B
			42	41	50	13	MOD 3*B
			44	43	50	13	MOD 2*B
			46	45	50	13	MOD 1*B
			48	47	50	13	MOD 0*B
GND		OUT	50	49	500mA		+VCC B
			52	51			

*Low-level active logic

One LSTTL load = 0.4 mA

Figure 2-11. User Interface Connector J2

PIN NUMBER				PIN NUMBER			
OUTPUT (LSTTL DRIVE)						OUTPUT (LSTTL DRIVE)	
INPUT (LSTTL LOADS)						INPUT (LSTTL LOADS)	
MNEMONIC							MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1**	55**	8	7	55**	1**	D3
D6	1**	55**	10	9	55**	1**	D2
D5	1**	55**	12	11	55**	1**	D1
D4	1**	55**	14	13	55**	1**	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX			36	35		1	IOEXP
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47		1	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

* Low-level active logic

** Only when the card is processor selected

One LSTTL load = 0.4 mA

Figure 2-12. STD Edge Connector

INTRODUCTION

The 7508 is a general purpose TTL I/O card designed primarily for use with industry standard I/O module mounting racks (see figure 3-1). The I/O module mounting rack is a standalone board that accepts plug-in I/O modules. The modules come in four types: AC input, AC output, DC input, and DC output. The modules can be placed in any position on the mounting rack, allowing for any number and combination of module types. The modules are optically isolated and insensitive to harsh environments and electrical noise.

The I/O module mounting rack is a convenient way to translate from TTL signals to industrial voltages while keeping high voltages and discrete heavy gauge wires isolated from the STD BUS. The entire system is modular, making it easy to set up, modify, and maintain. Figure 3-2 lists some of the features and benefits of the system. Figure 3-3, page 3-3, shows a block diagram of a complete control system. Figure 3-4, page 3-3, gives sources for hardware, and figure 3-5, page 3-4, shows schematics of four module types.

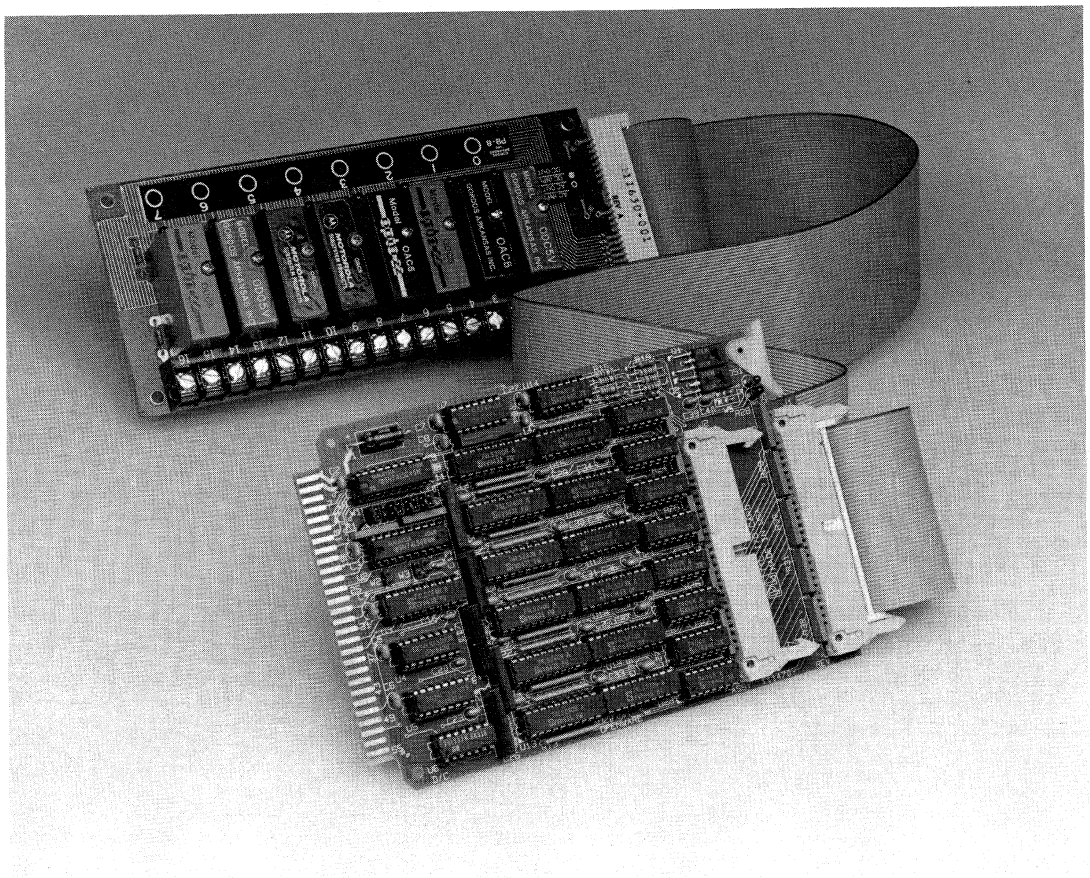


Figure 3-1. Industrial Interface System

FEATURES	BENEFITS
Industrial type barrier strip on mounting rack	Modules may be replaced without disturbing power wiring.
Plug-in modules	Meets Nema LCS 2-230. Power wiring need not be disconnected when changing modules.
Fully encapsulated modules	Provides immunity against adverse environments and increased thermal rating.
Individual plug-in fuses	Readily available fuses protect module and power wiring against short circuits.
LED status light for each module	Simplifies programming, setup, and troubleshooting.
2500 VAC isolation	Meets UL industrial specifications and VDE requirements.
8, 16, and 24 module racks available	Board size may be matched to system requirements.
Universal mounting racks	Allows use of any module in any position.
High voltage modules available	Allows operation on 240 VAC or up to 200 VDC.
UL Recognized	Safe, reliable.
Multisourced parts	Greater availability.
High industrial voltage and current away from STD BUS	Greater safety, reliability, and ease of maintenance.
No heavy gauge wires in STD BUS Card Rack	Ease of maintenance and installation.
Modules are opto-isolated	Immunity to fluctuations between digital ground and high-voltage ground.
Color-coded modules and module position markers	Reduces chances of using the wrong module or replacing with the wrong module.

Figure 3-2. Features and Benefits of the I/O Rack System

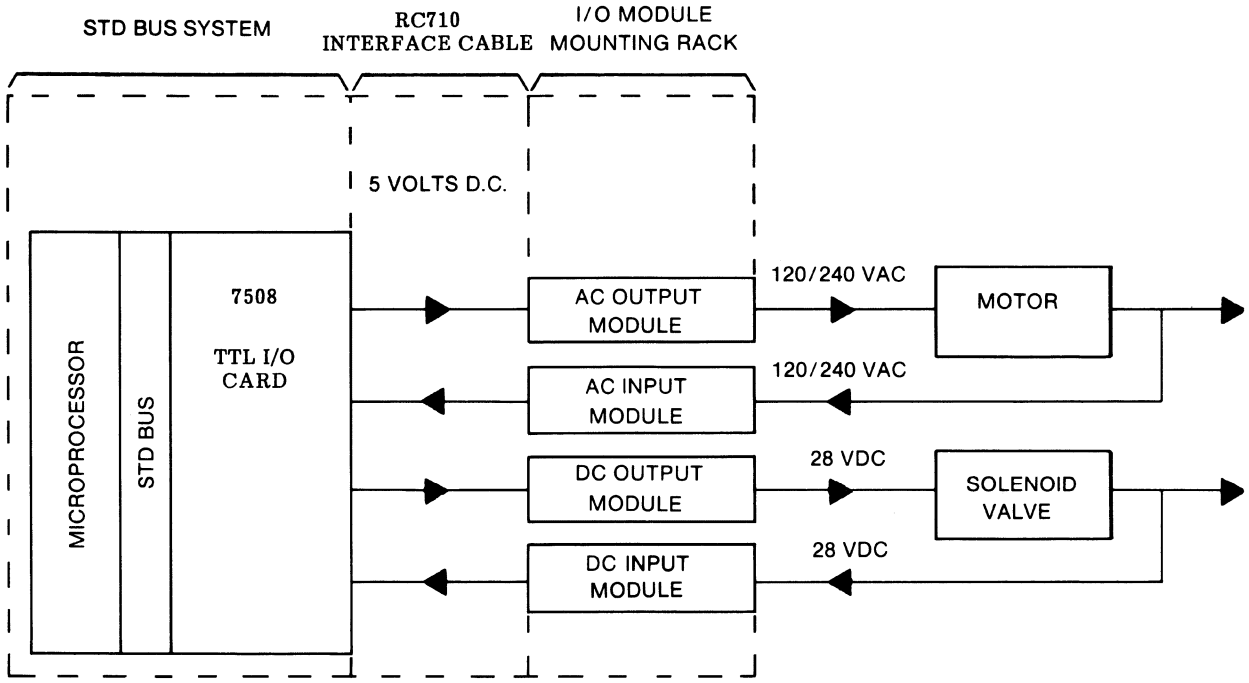


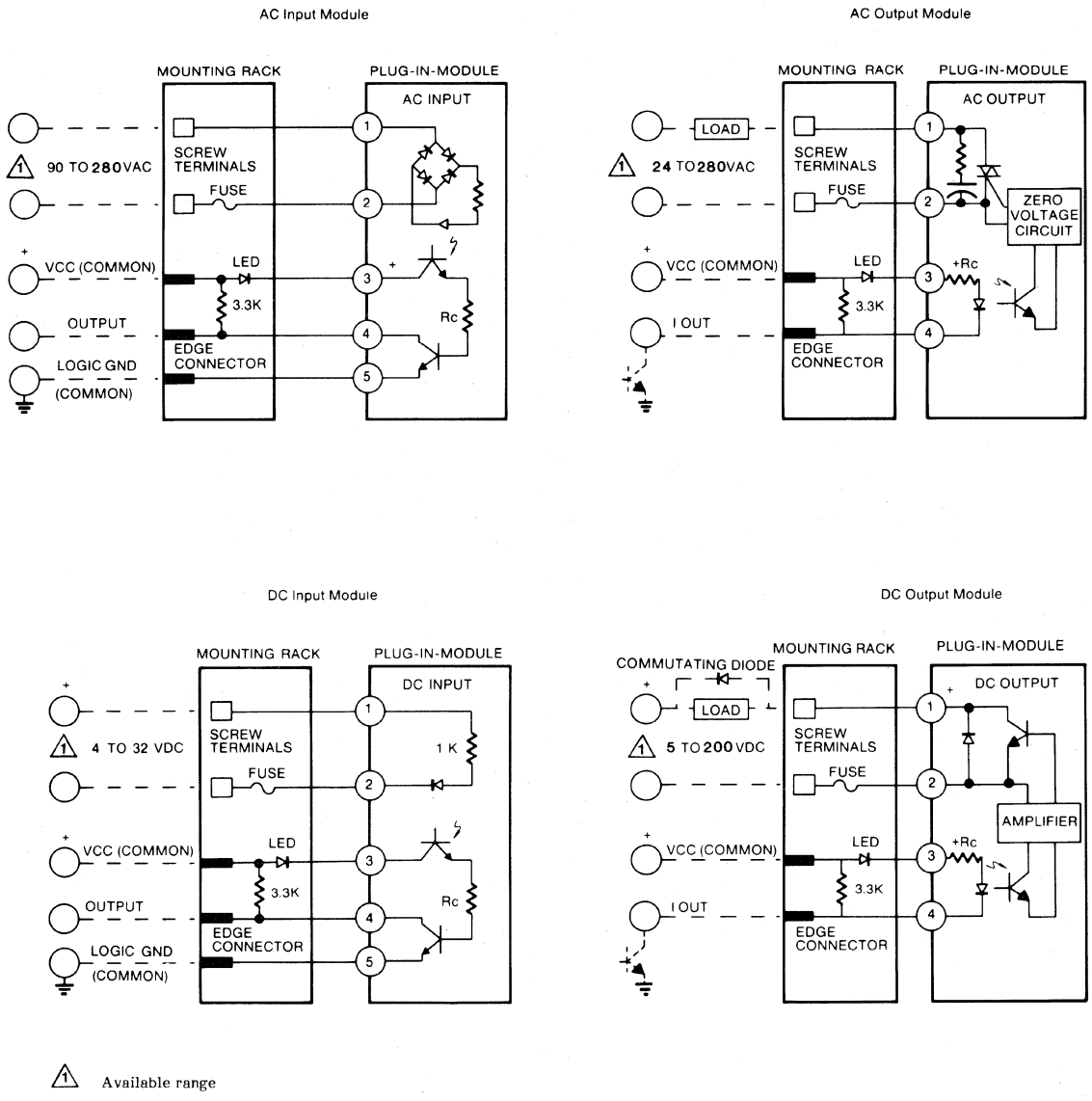
Figure 3-3. System Block Diagram

PART	MANUFACTURER
7508 RC710	Pro-Log Corporation
I/O Racks and Modules	Opto 22 Gordos Crydom Dutec
16 module addressable rack	Opto 22
32 module[1] adressable rack	Adatek

[1] These are addressable racks which allow daisy chaining a number of racks on one cable. By this method, hundreds of modules can be controlled by one interface card.

NOTE: This partial list is provided for convenience only and is not intended to recommend any manufacturer.

Figure 3-4. Manufacturers of I/O Racks



1 Available range

Figure 3-5. I/O Rack Module Schematics

I/O RACK INTERFACE

The 7508 TTL I/O card uses the industry standard I/O module bus to communicate with the I/O module mounting rack(s). The bus consists of 24 bidirectional data lines alternated with 24 ground lines, a switched +4.70 VDC (typical) power line, and a ground power line. The pinout of the interface connectors on the 7508 card directly matches the pinout of the I/O rack.

The pinout and typical schematic of an I/O rack are shown in figure 3-6. The I/O racks use a 50-pin card edge connector with pins on 0.1-inch centers. Pro-Log provides an RC710 interface cable which meets the requirements for connecting the 7508 card to the I/O rack. The I/O rack has a keying slot on its card edge connector. Keying the connector prevents it from being attached incorrectly.

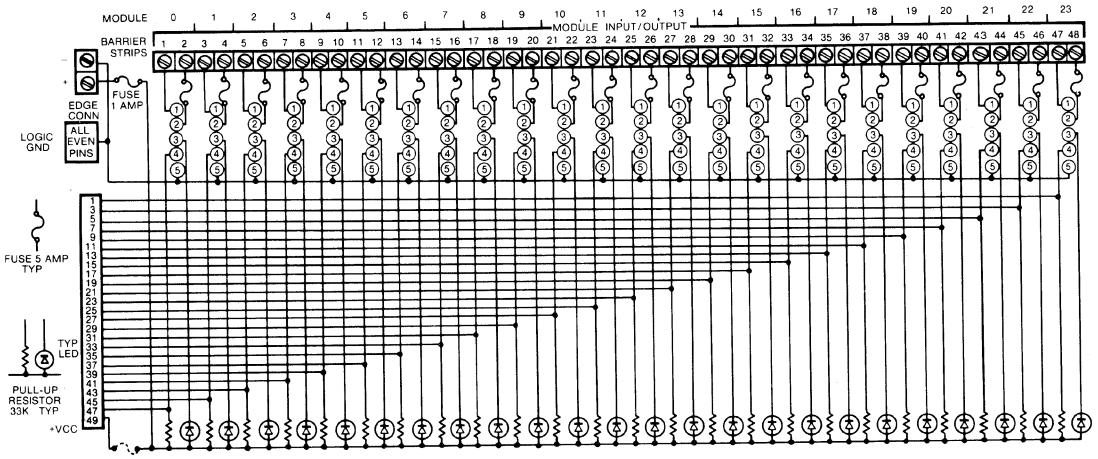


Figure 3-6. Typical I/O Rack Schematic

CONTROLLING I/O MODULES

To energize an AC or DC output module, simply write a one to the appropriate bit and port. The resulting low-level signal at the user interface connector will activate the module.

When an I/O line on the 7508 card is to be used to monitor an input AC or DC module, the associated latched bit of the output port must first be set to a one (reset). This is accomplished by writing a zero to the output port's bit.

Whenever writing to a port being used partly as input and partly as output, zeros should be written to the lines being used as inputs. Figure 2-7, page 2-10, shows a typical 7508 bidirectional I/O circuit.

GENERAL PURPOSE USE

The 7508 TTL I/O card can be used as a general purpose I/O card. The alternating signal and ground lines plus the filtering on the input ports offer a high degree of noise immunity in an I/O card. When using the 7508 for general purpose work, be sure to take into account the 27-microsecond delay of the input filters.

PARALLEL DATA COMMUNICATIONS

Each user interface connector on the 7508 provides three independent ports for data transfers between the CPU and peripheral devices. Under software control, two 8-bit bidirectional peripheral interface ports and up to 8 handshake lines can be configured. Refer to I/O Port Interface, page 2-9, and Specifications, page 2-11, for interface guidelines.

I/O RACK POWER

CAUTION

There is no current limiting on this line, so do not short it to ground. Connecting the cable backward may short this line to ground. Key the connector to avoid this possibility.

The I/O rack requires a +5V supply. The I/O rack has a two-position terminal block to which power can be connected directly or power can be supplied through the interface card. Line 49 of the 7508 card provides up to 500 mA at +4.70V (typical). It can be controlled via software or permanently connected directly to the +5V supply of the STD card rack. (See section 2, Module Rack Power, page 2-10.)

Software control of the I/O rack power line can be used to turn off the entire I/O rack, which may be useful in emergency situations.

Power must be applied to the rack for a self-test that writes to an output port and reads back at an input port. This is because the pullups for the open-collector output drivers are connected to the switched +5V (+VCC A and +VCC B). This switched power at the pullups eliminates a possible sneak current path through the pullups and a nonpowered rack.

Section 4

OPERATING SOFTWARE

INTRODUCTION

This section contains hardware-level subroutine modules to operate the 7508 as an I/O rack interface card.

The software in this section may be used without license from Pro-Log. Although tested and believed to be correct, this software is not represented to be free from errors, copyright infringement, or appropriate for any particular application.

These subroutines are written in STD instruction mnemonics. The coding forms are grouped at the end of this section.

Figure 4-13, page 4-14, is a program listing for a Z80 or 8085 system. Figure 4-14, page 4-18, is for an 8088 system.

MEMORY ADDRESSES

Full memory addresses are shown in the subroutine documentation. All memory and I/O port addresses are given in hexadecimal. They are the preferred addresses that allow the subroutines to work with those provided for other Series 7000 STD BUS cards.

If your system cannot use the memory addresses in the following software package, simply change the memory page addresses as required. Memory addresses that must be located in RAM are noted on the program coding forms. Other memory addresses shown are intended to be ROM locations, but may be RAM locations.

I/O PORT ADDRESSES

The 7508 I/O ports are assigned preferred hexadecimal addresses 50 through 57 for compatibility with other Series 7000 cards. Section 2 shows how to remap these addresses if necessary. This software can be used by simply changing the port addresses when loading the subroutines into your system.

SOFTWARE PACKAGE CONTENTS

The software package listed here can be used to drive a standard I/O module mounting rack from connector J1 on the 7508 card. To drive an addressed I/O module mounting rack (such as the Adatek RP32), consult the manufacturer of the mounting rack or Pro-Log Corporation.

Figure 4-1 lists the general purpose hardware-level subroutines provided to operate the 7508. These subroutines allow the card to communicate with the I/O module mounting rack on a bit-by-bit basis. With this software approach, you can turn on, turn off, or check the status of any one device without affecting any of the other devices connected to the I/O module mounting rack.

MODULE NAME	SUBROUTINE FUNCTION	SEE FIGURE
(INITIALIZE)	This subroutine sets all outputs to a predefined state. It also initializes all variables used by the other subroutines.	4-4
(COMPLEMENT BIT)	This subroutine complements one bit of the output lines.	4-5
(SET A BIT)	This subroutine sets one bit of the output lines.	4-6
(CLEAR A BIT)	This subroutine clears one bit of the output lines.	4-7
(TEST A BIT)	This subroutine checks the state of one of the output lines.	4-8
(TEST INPUT BIT)	This subroutine checks the state of one of the input lines.	4-9
(PWR ON)	Turns on module rack power.	4-10
(PWR OFF)	Turns off module rack power.	4-11
(WHICH LINE?)	This subroutine is used by the other subroutines to find the Port and Bit of the desired module.	4-12

Figure 4-1. Index of Subroutines

MEMORY MAPS

Figure 4-2 is a page map that shows subroutine locations for a Z80 or 8085 system.

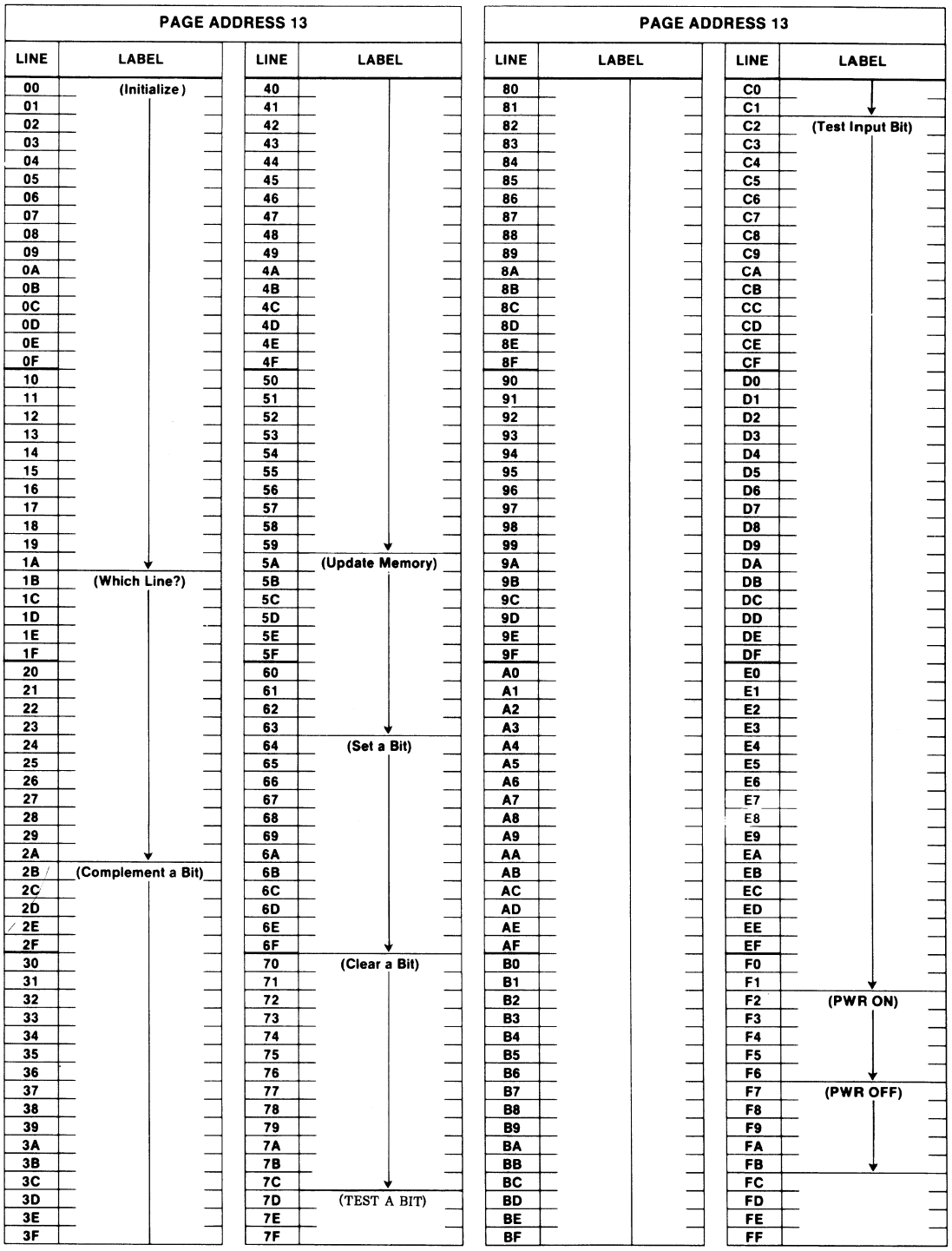


Figure 4-2. Subroutine Locations (Z80, 8085)

Figure 4-3 is a page map that shows subroutine locations for an 8088 system.

PAGE ADDRESS 13

LINE	LABEL	LINE	LABEL	LINE	LABEL	LINE	LABEL
00	(INITIALIZE)	40		80		C0	(SET A BIT)
01		41		81		C1	
02		42		82		C2	
03		43		83		C3	
04		44		84		C4	
05		45		85		C5	
06		46		86		C6	
07		47		87		C7	
08		48		88		C8	
09		49		89		C9	
0A		4A		8A		CA	
0B		4B		8B		CB	
0C		4C		8C		CC	
0D		4D		8D		CD	
0E		4E		8E		CE	
0F		4F		8F		CF	
10		50	(COMPLEMENT BIT)	90		D0	
11		51		91		D1	
12		52		92		D2	
13		53		93		D3	
14		54		94		D4	
15		55		95		D5	
16		56		96		D6	
17		57		97		D7	
18		58		98		D8	
19		59		99		D9	
1A		5A		9A		DA	
1B		5B		9B		DB	
1C		5C		9C		DC	
1D		5D		9D		DD	
1E		5E		9E		DE	
1F		5F		9F		DF	
20		60		A0	(UPDATE MEMORY)	E0	(CLEAR A BIT)
21		61		A1		E1	
22		62		A2		E2	
23		63		A3		E3	
24		64		A4		E4	
25		65		A5		E5	
26		66		A6		E6	
27		67		A7		E7	
28		68		A8		E8	
29		69		A9		E9	
2A		6A		AA		EA	
2B		6B		AB		EB	
2C		6C		AC		EC	
2D		6D		AD		ED	
2E		6E		AE		EE	
2F		6F		AF		EF	
30	(WHICH LINE?)	70		B0		F0	
31		71		B1		F1	
32		72		B2		F2	
33		73		B3		F3	
34		74		B4		F4	
35		75		B5		F5	
36		76		B6		F6	
37		77		B7		F7	
38		78		B8		F8	
39		79		B9		F9	
3A		7A		BA		FA	
3B		7B		BB		FB	
3C		7C		BC		FC	
3D		7D		BD		FD	
3E		7E		BE		FE	
3F		7F		BF		FF	

Figure 4-3. Subroutine Locations (8088)

PAGE ADDRESS 14

LINE	LABEL	LINE	LABEL	LINE	LABEL	LINE	LABEL
00	(TEST A BIT)	40		80		C0	
01		41		81		C1	
02		42		82		C2	
03		43		83		C3	
04		44		84		C4	
05		45		85		C5	
06		46		86		C6	
07		47		87		C7	
08		48		88		C8	
09		49		89		C9	
0A		4A		8A		CA	
0B		4B		8B		CB	
0C		4C		8C		CC	
0D		4D		8D		CD	
0E		4E		8E		CE	
0F		4F		8F		CF	
10		50		90		D0	
11		51		91		D1	
12		52		92		D2	
13		53		93		D3	
14		54		94		D4	
15		55		95		D5	
16		56		96		D6	
17		57		97		D7	
18		58		98		D8	
19		59		99		D9	
1A		5A		9A		DA	
1B		5B		9B		DB	
1C		5C		9C		DC	
1D		5D		9D		DD	
1E		5E		9E		DE	
1F		5F		9F		DF	
20		60		A0		E0	
21		61		A1		E1	
22		62		A2		E2	
23		63		A3		E3	
24		64		A4		E4	
25		65		A5		E5	
26		66		A6		E6	
27		67		A7		E7	
28		68		A8		E8	
29		69		A9		E9	
2A		6A		AA		EA	
2B		6B		AB		EB	
2C		6C		AC		EC	
2D		6D		AD		ED	
2E		6E		AE		EE	
2F		6F		AF		EF	
30		70	(TEST INPUT BIT)	B0	(PWR ON)	F0	
31		71		B1		F1	
32		72		B2		F2	
33		73		B3		F3	
34		74		B4		F4	
35		75		B5		F5	
36		76		B6		F6	
37		77		B7		F7	
38		78		B8	(PWR OFF)	F8	
39		79		B9		F9	
3A		7A		BA		FA	
3B		7B		BB		FB	
3C		7C		BC		FC	
3D		7D		BD		FD	
3E		7E		BE		FE	
3F		7F		BF		FF	

Figure 4-3. Subroutine Locations (8088) (Continued)

(INITIALIZE) SUBROUTINE

This subroutine sets all of the outputs from connector J1 on the 7508 card to a predefined state. It also initializes all variables used by the other subroutines.

To use this routine:

1. Select three consecutive memory locations in RAM memory and put the first address in locations 1301 and 1302 hex. These three RAM locations are used by the other subroutines in this package.

2. Put the initial state of modules 16-23 into location 1304 (1 = on, 0 = off). Refer to I/O Port Bit Assignments, page 2-5 for bit-to-module identification (D0 = MOD 23, D7 = MOD 16).

3. Put the initial state of modules 8-15 into location 1308 (D0=MOD 15, D7= MOD 8).

4. Put the initial state of modules 0-7 into location 130C (D0=MOD 7, D7=MOD 0).

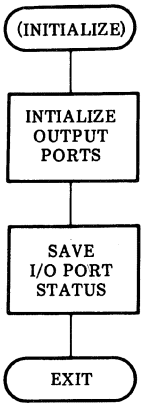


Figure 4-4. (INITIALIZE) Flowchart

(COMPLEMENT BIT) SUBROUTINE

This routine accepts a hex value in the accumulator. This value corresponds to the I/O module to be complemented, i.e., 00 hex = MOD 0, 17 hex = MOD 23). If the I/O module number is out of range, the carry flag is set.

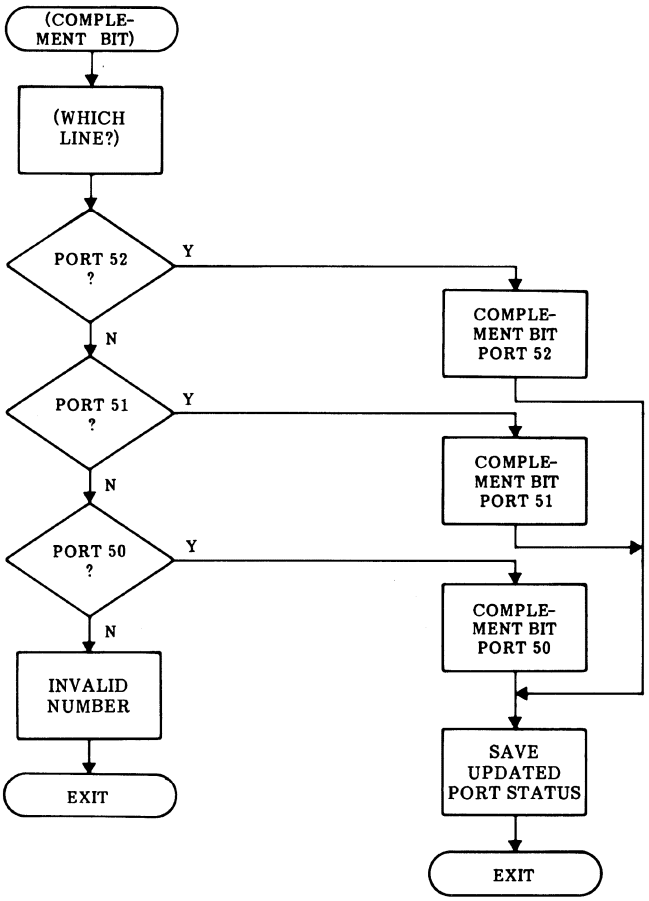


Figure 4-5. (COMPLEMENT BIT) Flowchart

(SET A BIT) SUBROUTINE

This routine accepts a hex value in the accumulator. This value corresponds to the I/O module to be turned on. If the I/O module number is out of range, the carry flag is set.

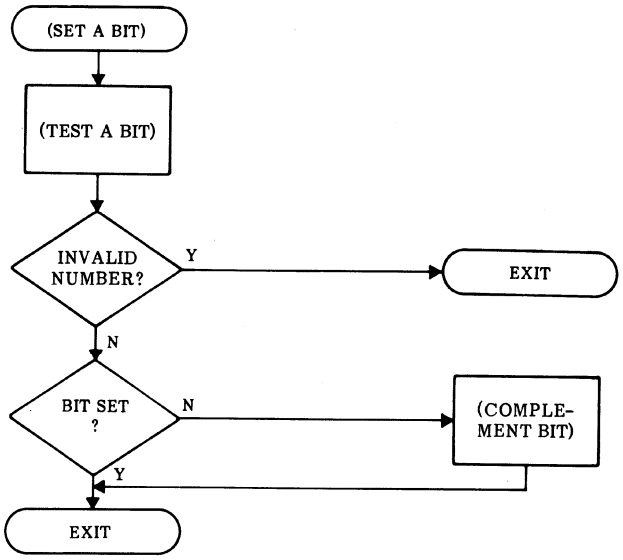


Figure 4-6. (SET A BIT) Flowchart

(CLEAR A BIT) SUBROUTINE

This routine accepts a hex value in the accumulator. This value corresponds to the I/O module to be turned off. If the I/O module number is out of range, the carry flag is set.

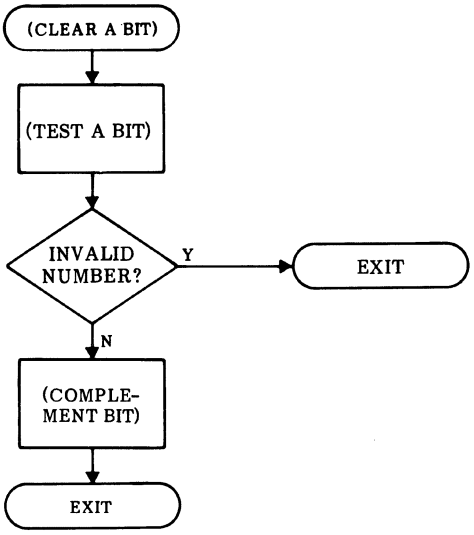


Figure 4-7. (CLEAR A BIT) Flowchart

(TEST A BIT) SUBROUTINE

The (TEST A BIT) subroutine is used to check the state of an output module. It is also used by the (TEST INPUT BIT) subroutine. (TEST A BIT) accepts a hex value in the accumulator. This value corresponds to the output module to be tested. If the I/O module number is out of range, the carry flag is set. It returns with the sign flag=0 if there was no change and S=1 if the addressed module has changed since the last test. The Z flag equals zero if the bit is set and Z equals one if the input bit is clear.

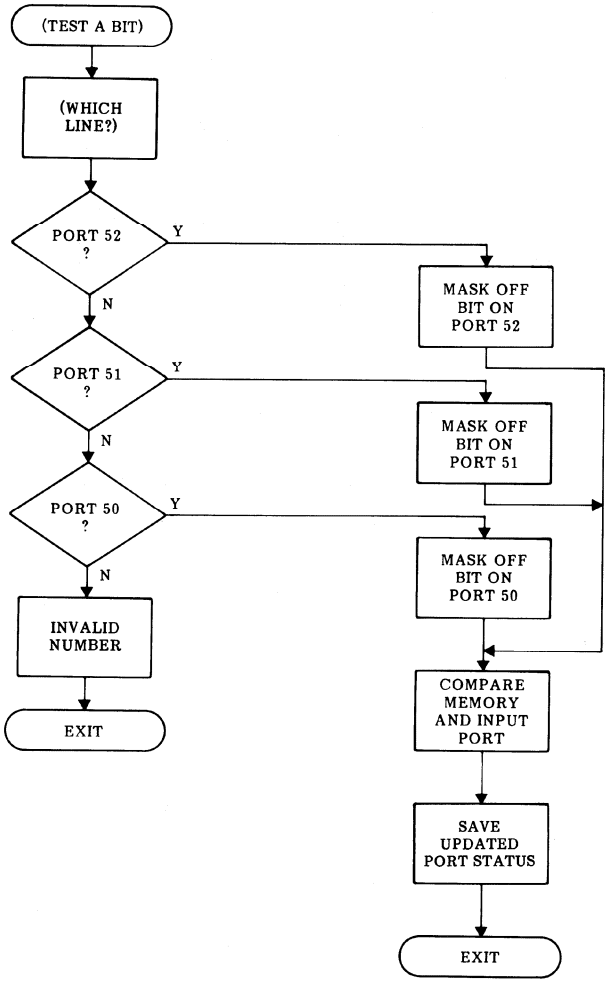


Figure 4-8. (TEST A BIT) Flowchart

(TEST INPUT BIT) SUBROUTINE

The (TEST INPUT BIT) subroutine is used to input the state of an input module. This routine accepts a hex value in the accumulator that corresponds to the input module to be tested. If the I/O module number is out of range, the carry flag is set. It returns with the sign flag=0 if there was no change and S=1 if the addressed module has changed since the last test. The Z flag equals zero if the bit is set and Z equals one if the input bit is clear.

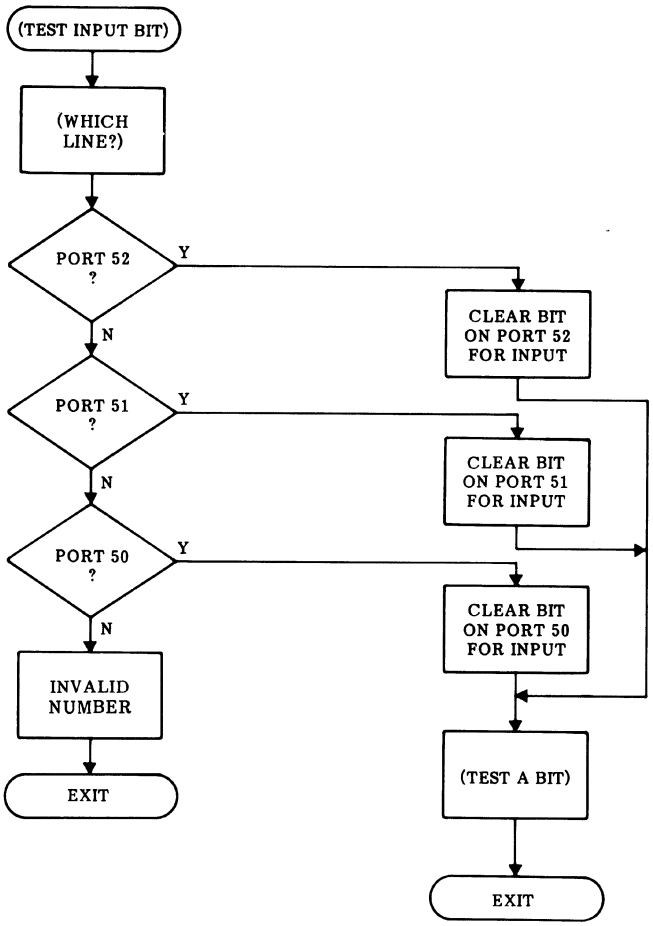


Figure 4-9. (TEST INPUT BIT) Flowchart

(PWR ON) SUBROUTINE

This routine turns on the power to the I/O module rack (refer to Module Rack Power, page 2-10).

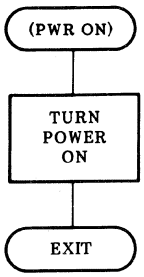


Figure 4-10. (PWR ON) Flowchart

(PWR OFF) SUBROUTINE

This routine turns off the power to the I/O module rack (refer to Module Rack Power, page 2-10).

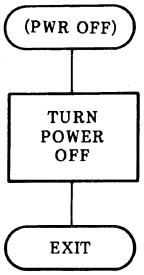


Figure 4-11. (PWR OFF) Flowchart

(WHICH LINE?) SUBROUTINE

This is a support routine used by other routines to calculate the correct port and bit for each module. The routine can be used alone for other purposes. It converts a number in the accumulator into the correct port and bit numbers. This routine is not limited to the 24-position rack; it can calculate the correct port and bit for up to 256 modules.

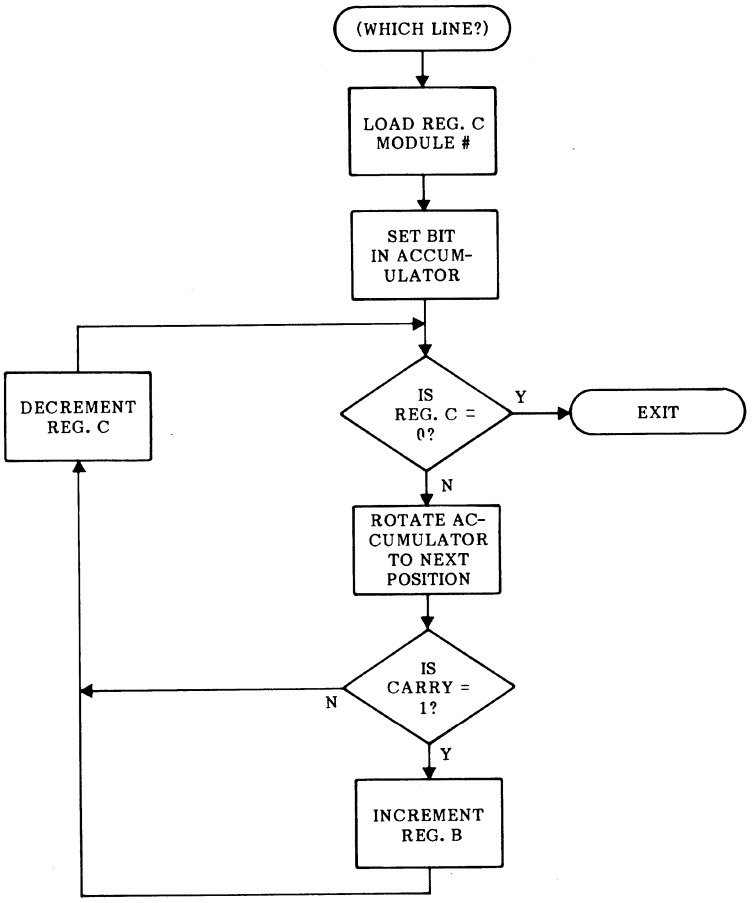


Figure 4-12. (WHICH LINE?) Flowchart

```
ADRdata!      LABEL       !INSTR !     MODIFIER     !            COMMENTS
-------------------------------------------------------------------------------
1300 21!(INITIALIZE)      !LDPI  !HL                !TURN OFF ALL OF THE MODULES
  01 70!                  ! ---- !2070 hex          !   AT USER INTERFACE CONN. J1.
  02 20!                  ! ---- !                  !HL= 1st port's bit status.
  03 3E!                  !LDAI  !                  !Set MOD 16*A   thru MOD 23*A
  04 00!                  ! ---- !00 hex            !   via as shipped port.
  05 D3!                  !OPA   !                  !
  06 50!                  ! ---- !50 hex            !
  07 3E!                  !LDAI  !                  !Set MOD 8*A    thru MOD 15*A
  08 00!                  ! ---- !00 hex            !   via as shipped port.
  09 D3!                  !OPA   !                  !
  0A 51!                  ! ---- !51 hex            !
  0B 3E!                  !LDAI  !                  !Set MOD 0*A    thru MOD 7*A
  0C 00!                  ! ---- !00 hex            !   via as shipped port.
  0D D3!                  !OPA   !                  !
  0E 52!                  ! ---- !52 hex            !
  0F DB!                  !IPA   !                  !Input the as shipped ports of
1310 50!                  ! ---- !50 hex            !  user interface conn. J1 and
  11 77!                  !STAN  !(HL)              !  save the bit status in
  12 23!                  !ICP   !HL                !  memory. note:
  13 DB!                  !IPA   !                  !  0 = I/O line high, module off
  14 51!                  ! ---- !51 hex            !  1 = I/O line low, module on.
  15 77!                  !STAN  !(HL)              !
  16 23!                  !ICP   !HL                !
  17 DB!                  !IPA   !                  !
  18 52!                  ! ---- !52 hex            !
  19 77!                  !STAN  !(HL)              !
  1A C9!   ----------     !RTS   !UN                !Return.
131B 4F!(WHICH LINE?)     !LDR   !C,A               !CONVERT THE MODULE NUMBER IN
  1C 3E!                  !LDAI  !                  !  REG. A TO A BIT POSITION AT
  1D 80!                  ! ---- !80 hex            !  USER INTER. CONN. J1 OR J2.
  1E 06!                  !LDRI  !B                 !  REGISTER A WILL = BIT
  1F 01!                  ! ---- !01 hex            !  REGISTER B WILL = PORT:
1320 0C!                  !ICR   !C                 !   01=1st PORT, 02=2nd PORT,
1321 0D!LOOP              !DCR   !C                 !   03=3rd PORT
  22 C8!                  !RTS   !ZERO              !Return with bit and port.
  23 0F!                  !RRA   !                  !Rotate to the next bit
  24 D2!                  !JP    !NO CARRY          !   position.
  25 21!                  ! ---- !LOOP              !
  26 13!                  ! ---- !                  !
  27 04!                  !ICR   !B                 !Increment register B (port)
  28 C3!                  !JP    !UN                !   until the carry bit is set.
  29 21!                  ! ---- !LOOP              !
  2A 13!   ----------     ! ---- !                  !
132B CD!(COMPLEMENT BIT)  !JS    !UN                !DETERMINE THE OUTPUT MODULE
  2C 1B!                  ! ---- !(WHICH LINE?)     !   STATUS AT USER INTERFACE
  2D 13!                  ! ---- !                  !   CONN. J1 AND COMPLEMENT IT.
  2E 21!                  !LDPI  !HL                !Set the pointer to the memory
  2F 72!                  ! ---- !2072 hex          !   location of the third port's
1330 20!                  ! ---- !                  !   bit status.
  31 05!                  !DCR   !B                 !Find the correct port routine
  32 CA!                  !JP    !ZERO              !   for the bit (I/O line) to
  33 54!                  ! ---- !THIRD PORT A      !   be complemented.
  34 13!                  ! ---- !                  !
  35 2B!                  !DCP   !HL                !CONN.      PORT *     BIT STATUS
  36 05!                  !DCR   !B                 !-----  ------------ ----------
  37 CA!                  !JP    !ZERO              !       PORT 50  1ST     BSA
  38 4B!                  ! ---- !SECOND PORT A     ! J1    PORT 51  2ND     BSA+1
  39 13!                  ! ---- !                  !       PORT 52  3RD     BSA+2
  3A 2B!                  !DCP   !HL                !
  3B 05!                  !DCR   !B                 !       PORT 54  1ST     BSA+3
  3C CA!                  !JP    !ZERO              ! J2    PORT 55  2ND     BSA+4
  3D 42!                  ! ---- !FIRST PORT A      !       PORT 56  3RD     BSA+5
  3E 13!                  ! ---- !                  !
  3F 00!                  !NOP   !                  !       *=AS SHIPPED

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```

Figure 4-13. Program Listing for Subroutines (Z80, 8085)

```
ADRdata!     LABEL       !INSTR !    MODIFIER    !          COMMENTS
-------------------------------------------------------------------------------
1340 37!                 !SEC   !                !Invalid bit number. Set carry
  41 C9!   ----------    !RTS   !UN              !   bit to 1 and return.
1342 47!FIRST PORT A     !LDR   !B,A             !Update port 50 (as shipped)
  43 DB!                 !IPA   !                !   at user interface conn. J1
  44 50!                 ! ---- !50 hex          !   and update the bit status
  45 A8!                 !XRA   !B               !   in memory.
  46 D3!                 !OPA   !                !
  47 50!                 ! ---- !50 hex          !
  48 C3!                 !JP    !UN              !
  49 5A!                 ! ---- !(UPDATE MEMORY) !
  4A 13!   ----------    ! ---- !                !
134B 47!SECOND PORT A    !LDR   !B,A             !Update port 51 (as shipped)
  4C DB!                 !IPA   !                !   at user interface conn. J1
  4D 51!                 ! ---- !51 hex          !   and update the bit status
  4E A8!                 !XRA   !B               !   in memory.
  4F D3!                 !OPA   !                !
1350 51!                 ! ---- !51 hex          !
  51 C3!                 !JP    !UN              !
  52 5A!                 ! ---- !(UPDATE MEMORY) !
  53 13!   ----------    ! ---- !                !
1354 47!THIRD PORT A     !LDR   !B,A             !Update port 52 (as shipped)
  55 DB!                 !IPA   !                !   at user interface conn. J1
  56 52!                 ! ---- !52 hex          !   and update the bit status
  57 A8!                 !XRA   !B               !   in memory.
  58 D3!                 !OPA   !                !
  59 52!                 ! ---- !52 hex          !
135A A0!(UPDATE MEMORY)  !ANA   !B               !Mask all but the changed bit.
  5B 4F!                 !LDR   !C,A             !Save the changed bit in reg. C.
  5C 78!                 !LDA   !B               !Use reg. B as bit mask.
  5D 2F!                 !CMA   !                !
  5E 47!                 !LDR   !B,A             !
  5F 7E!                 !LDAN  !(HL)            !
1360 A0!                 !ANA   !B               !Mask out the changed bit.
  61 B1!                 !ORA   !C               !OR in the changed bit.
  62 77!                 !STAN  !(HL)            !Store new bit status in memory.
  63 C9!   ----------    !RTS   !UN              !Return.
1364 47!(SET A BIT)      !LDR   !B,A             !DETERMINE THE OUTPUT MODULE TO
  65 C5!                 !PSP   !BC              !   BE TURNED ON (I/O LINE LOW).
  66 CD!                 !JS    !UN              !   TEST THE BIT THAT CONTROLS
  67 7D!                 ! ---- !(TEST A BIT)    !   THE STATUS OF THE MODULE,
  68 13!                 ! ---- !                !   AND IF NOT SET, SET IT.
  69 C1!                 !PLP   !BC              !
  6A D8!                 !RTS   !CARRY           !Set C=1 and return if an
  6B 78!                 !LDA   !B               !   invalid bit number.
  6C CC!                 !JS    !ZERO            !If the bit is not already set,
  6D 2B!                 ! ---- !(COMPLEMENT BIT)!   complement it and update the
  6E 13!                 ! ---- !                !   bit status in memory.
  6F C9!   ----------    !RTS   !UN              !Return.
1370 47!(CLEAR A BIT)    !LDR   !B,A             !DETERMINE THE OUTPUT MODULE TO
  71 C5!                 !PSP   !BC              !   BE TURNED OFF (I/O LINE HI).
  72 CD!                 !JS    !UN              !   TEST THE BIT THAT CONTROLS
  73 7D!                 ! ---- !(TEST A BIT)    !   THE STATUS OF THE MODULE,
  74 13!                 ! ---- !                !   AND IF NOT CLEARED,CLEAR IT.
  75 C1!                 !PLP   !BC              !
  76 D8!                 !RTS   !CARRY           !Set C=1 and return if an
  77 78!                 !LDA   !B               !   invalid bit number.
  78 C4!                 !JS    !NOT ZERO        !If the bit is not already
  79 2B!                 ! ---- !(COMPLEMENT BIT)!   cleared, complement it and
  7A 13!                 ! ---- !                !   update bit status in memory.
  7B C9!   ----------    !RTS   !UN              !Return.
  7C FF!                 !      !                !
137D CD!(TEST A BIT)     !JS    !UN              !DETERMINE THE HIGH/LOW STATUS
  7E 1B!                 ! ---- !(WHICH LINE?)   !   OF AN I/O LINE AT THE USER
  7F 13!                 ! ---- !                !   INTERFACE CONN.

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Figure 4-13. (Continued)

```
ADRdata!     LABEL          !INSTR !    MODIFIER     !          COMMENTS
-------------------------------------------------------------------------------
1380 21!                    !LDPI  !HL                !Set the pointer to the third
  81 72!                    ! ---- !2072 hex          !   port's bit status.
  82 20!                    ! ---- !                  !
  83 05!                    !DCR   !B                 !Find the correct port routine
  84 CA!                    !JP    !ZERO              !   for the bit to be checked.
  85 A0!                    ! ---- !THIRD PORT B      !
  86 13!                    ! ---- !                  !
  87 2B!                    !DCP   !HL                !
  88 05!                    !DCR   !B                 !
  89 CA!                    !JP    !ZERO              !
  8A 9A!                    ! ---- !SECOND PORT B     !
  8B 13!                    ! ---- !                  !
  8C 2B!                    !DCP   !HL                !
  8D 05!                    !DCR   !B                 !
  8E CA!                    !JP    !ZERO              !
  8F 94!                    ! ---- !FIRST PORT B      !
1390 13!                    ! ---- !                  !
  91 00!                    !NOP   !                  !
  92 37!                    !SEC   !                  !Invalid bit number. Set the
  93 C9!  ----------        !RTS   !UN                !   carry bit to 1 and return.
1394 47!FIRST PORT B        !LDR   !B,A               !Save the mask.
  95 DB!                    !IPA   !                  !Input the port (as shipped) of
  96 50!                    ! ---- !50 hex            !   the bit to be checked (J1).
  97 C3!                    !JP    !UN                !Update the bit status in
  98 A3!                    ! ---- !UPDATE FLAGS      !   memory.
  99 13!  ----------        ! ---- !                  !
139A 47!SECOND PORT B       !LDR   !B,A               !Save the mask.
  9B DB!                    !IPA   !                  !Input the port (as shipped) of
  9C 51!                    ! ---- !51 hex            !   the bit to be checked (J1).
  9D C3!                    !JP    !UN                !Update the bit status in
  9E A3!                    ! ---- !UPDATE FLAGS      !   memory.
  9F 13!  ----------        ! ---- !                  !
13A0 47!THIRD PORT B        !LDR   !B,A               !Save the mask.
  A1 DB!  ----------        !IPA   !                  !Input the port (as shipped) of
  A2 52!                    ! ---- !52 hex            !   the bit to be checked (J1).
13A3 A0!UPDATE FLAGS        !ANA   !B                 !SET FLAG STATUS:
  A4 F5!                    !PSP   !AF                !   P=0 : NO CHANGE
  A5 7E!                    !LDAN  !(HL)              !   P=1 : BIT HAS CHANGED SINCE
  A6 A0!                    !ANA   !B                 !         LAST TEST.
  A7 4F!                    !LDR   !C,A               !   Z=0 : BIT IS SET (I/O LINE
  A8 F1!                    !PLP   !AF                !         IS LOW).
  A9 F5!                    !PSP   !AF                !   Z=1 : BIT IS CLEAR (I/O LINE
  AA C5!                    !PSP   !BC                !         IS HIGH).
  AB CD!                    !JS    !UN                !Update memory to the present
  AC 5A!                    ! ---- !(UPDATE MEMORY)   !   bit status.
  AD 13!                    ! ---- !                  !
  AE C1!                    !PLP   !BC                !Put old data back in reg. A.
  AF 79!                    !LDA   !C                 !
13B0 C1!                    !PLP   !BC                !Put new data and flags in BC.
  B1 A8!                    !XRA   !B                 !XOR old and new data.Z0=change.
  B2 F5!                    !PSP   !AF                !Put "change" flag on stack.
  B3 79!                    !LDA   !C                 !Put zero flag in reg. A.
  B4 E6!                    !ANAI  !                  !Mask off the sign bit.
  B5 7F!                    ! ---- !7F hex            !
  B6 C1!                    !PLP   !BC                !Pull "change" flag into reg. C.
  B7 47!                    !LDR   !B,A               !Put the zero flag into reg. B.
  B8 79!                    !LDA   !C                 !Complement "change" flag and
  B9 2F!                    !CMA   !                  !   rotate into sign position.
  BA 07!                    !RLA   !                  !
  BB E6!                    !ANAI  !                  !
  BC 80!                    ! ---- !80 hex            !
  BD B0!                    !ORA   !B                 !OR "change" and "bit" flags.
  BE 4F!                    !LDR   !C,A               !Put the flags into reg. C.
  BF C5!                    !PSP   !BC                !Set the flag register.

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Figure 4-13. (Continued)

```
ADRdata!      LABEL          !INSTR !    MODIFIER     !          COMMENTS
-------------------------------------------------------------------------------
13C0 F1!                     !PLP   !AF                !Set the flag bit.
  C1 C9!   ----------        !RTS   !UN                !Return.
13C2 F5!(TEST INPUT BIT)     !PSP   !AF                !CLEAR THE LATCHED BIT OF THE
  C3 CD!                     !JS    !UN                !   I/O LINE AT THE USER INTER.
  C4 1B!                     ! ---- !(WHICH LINE?)     !   CONN. WHICH IS  TO BE USED
  C5 13!                     ! ---- !                  !   AS AN INPUT. INPUT THE PORT,
  C6 2F!                     !CMA   !                  !   AND UPDATE BIT STATUS.
  C7 05!                     !DCR   !B                 !Find the correct port routine
  C8 CA!                     !JP    !ZERO              !   for the bit to be  checked.
  C9 E8!                     ! ---- !THIRD PORT C      !
  CA 13!                     ! ---- !                  !
  CB 05!                     !DCR   !B                 !
  CC CA!                     !JP    !ZERO              !
  CD DF!                     ! ---- !SECOND PORT C     !
  CE 13!                     ! ---- !                  !
  CF 05!                     !DCR   !B                 !
13D0 CA!                     !JP    !ZERO              !
  D1 D6!                     ! ---- !FIRST PORT C      !
  D2 13!                     ! ---- !                  !
  D3 F1!                     !PLP   !AF                !
  D4 37!                     !SEC   !                  !Invalid bit number. Set carry
  D5 C9!   ----------        !RTS   !UN                !   bit to 1 and return.
13D6 47!FIRST PORT C         !LDR   !B,A               !Clear the bit at J1 port 50
  D7 DB!                     !IPA   !                  !   (as shipped) used as input.
  D8 50!                     ! ---- !50 hex            !
  D9 A0!                     !ANA   !B                 !
  DA D3!                     !OPA   !                  !
  DB 50!                     ! ---- !50 hex            !
  DC C3!                     !JP    !UN                !
  DD EE!                     ! ---- !PULL              !
  DE 13!   ----------        ! ---- !                  !
13DF 47!SECOND PORT C        !LDR   !B,A               !Clear the bit at J1 port 51
13E0 DB!                     !IPA   !                  !   (as  shipped) used as input.
  E1 51!                     ! ---- !51 hex            !
  E2 A0!                     !ANA   !B                 !
  E3 D3!                     !OPA   !                  !
  E4 51!                     ! ---- !51 hex            !
  E5 C3!                     !JP    !UN                !
  E6 EE!                     ! ---- !PULL              !
  E7 13!   ----------        ! ---- !                  !
13E8 47!THIRD PORT C         !LDR   !B,A               !Clear the bit at J1 port 52
  E9 DB!                     !IPA   !                  !   (as shipped) used as input.
  EA 52!                     ! ---- !52 hex            !
  EB A0!                     !ANA   !B                 !
  EC D3!                     !OPA   !                  !
  ED 52!                     ! ---- !52 hex            !
13EE F1!PULL                 !PLP   !AF                !Restore registers.
  EF C3!                     !JP    !UN                !Check the status of the input
13F0 7D!                     ! ---- !(TEST A BIT)      !   module and update bit
  F1 13!   ----------        ! ---- !                  !   status.
13F2 3E!(PWR ON)             !LDAI  !                  !TURN ON MODULE RACK POWER
  F3 00!                     ! ---- !00 hex            !   +VCC A.
  F4 D3!                     !OPA   !                  !
  F5 53!                     ! ---- !53 hex            !
  F6 C9!   ----------        !RTS   !UN                !Return.
13F7 3E!(PWR OFF)            !LDAI  !                  !TURN OFF MODULE RACK POWER
  F8 80!                     ! ---- !80 hex            !   +VCC(1).
  F9 D3!                     !OPA   !                  !
  FA 53!                     ! ---- !53 hex            !
  FB C9!   ----------        !RTS   !UN                !Return.
  FC FF!                     !      !                  !
  FD FF!                     !      !                  !
  FE FF!                     !      !                  !
  FF FF!                     !      !                  !

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Figure 4-13. (Continued)

```
ADRdata!     LABEL      !INSTR !     MODIFIER    !          COMMENTS
-------!----------------!------!-----------------!-----------------------------
1300 C7!(INITIALIZE)    !LDPI  !HL               !TURN OFF ALL OF THE MODULES
  01 C3!                ! --   !2070 hex         !  AT USER INTERFACE CONN J1.
  02 70!                ! --   !                 !HL=1st port's bit status.
  03 20!                ! --   !                 !
  04 B0!                !LDAI  !                 !Set MOD 16*A thru MOD 23*A
  05 00!                ! --   !00 hex           !  via as shipped port.
  06 E6!                !OPA   !                 !
  07 50!                ! --   !50 hex           !
  08 B0!                !LDAI  !                 !Set MOD 8*A thru MOD 15*A
  09 00!                ! --   !00 hex           !  via as shipped port.
  0A E6!                !OPA   !                 !
  0B 51!                ! --   !51 hex           !
  0C B0!                !LDAI  !                 !Set MOD 0*A thru MOD 7*A
  0D 00!                ! --   !00 hex           !  via as shipped port.
  0E E6!                !OPA   !                 !
  0F 52!                ! --   !52 hex           !
1310 E4!                !IPA   !                 !Input the as shipped ports of
  11 50!                ! --   !50 hex           !  user interface conn J1 and
  12 88!                !STAN  !(HL)             !  save the bit status in
  13 07!                ! --   !                 !  memory, note:
  14 43!                !ICP   !HL               !  0=I/O line high, module off
  15 E4!                !IPA   !                 !  1=I/O line low, module on.
  16 51!                ! --   !51 hex           !
  17 88!                !STAN  !(HL)             !
  18 07!                ! --   !                 !
  19 43!                !ICP   !HL               !
  1A E4!                !IPA   !                 !
  1B 52!                ! --   !52 hex           !
  1C 88!                !STAN  !(HL)             !
  1D 07!                ! --   !                 !
  1E C3!                !RTS   !UN               !RETURN
  1F FF!                !      !                 !
1320 FF!                !      !                 !
  21 FF!                !      !                 !
  22 FF!                !      !                 !
  23 FF!                !      !                 !
  24 FF!                !      !                 !
  25 FF!                !      !                 !
  26 FF!                !      !                 !
  27 FF!                !      !                 !
  28 FF!                !      !                 !
  29 FF!                !      !                 !
  2A FF!                !      !                 !
  2B FF!                !      !                 !
  2C FF!                !      !                 !
  2D FF!                !      !                 !
  2E FF!                !      !                 !
  2F FF!                !      !                 !
1330 8A!(WHICH LINE?)   !LDR   !C,A              !CONVERT THE MODULE NUMBER IN
  31 C8!                ! --   !                 !  REG. A TO A BIT POSITION AT
  32 B0!                !LDAI  !                 !  USER INTER. CONN. J1 OR J2.
  33 80!                ! --   !80 hex           !  REGISTER A WILL = BIT
  34 B5!                !LDRI  !B                !  REGISTER B WILL = PORT:
  35 01!                ! --   !01 hex           !   01=1st PORT, 02=2nd PORT,
  36 FE!                !ICR   !C                !   03=3rd PORT
  37 C1!                ! --   !                 !
  38 FE!LOOP            !DCR   !C                !
  39 C9!                ! --   !                 !
  3A 74!                !JPRS  !ZERO             !Return with bit and port.
  3B 08!                ! --   !R1               !
  3C D0!                !RRA   !                 !Rotate to the next bit
  3D C8!                ! --   !                 !  position.
  3E 73!                !JPRS  !NO CARRY         !
  3F F8!                ! --   !LOOP             !
```

Figure 4-14. Program Listing for Subroutines (8088)

```
ADRdata!     LABEL       !INSTR !     MODIFIER    !           COMMENTS
-------!-----------------!------!-----------------!-----------------------------
1340 FE!                 !ICR   !B                !Increment register B (port)
  41 C5!                 ! --   !                 !  until the carry bit is set.
  42 EB!                 !JPRS  !UN               !
  43 F4!                 ! --   !LOOP             !
  44 C3!R1               !RTS   !UN               !RETURN
  45 FF!                 !      !                 !
  46 FF!                 !      !                 !
  47 FF!                 !      !                 !
  48 FF!                 !      !                 !
  49 FF!                 !      !                 !
  4A FF!                 !      !                 !
  4B FF!                 !      !                 !
  4C FF!                 !      !                 !
  4D FF!                 !      !                 !
  4E FF!                 !      !                 !
  4F FF!                 !      !                 !
1350 E8!(COMPLEMENT BIT)!JSR   !UN               !DETERMINE THE OUTPUT MODULE
  51 DD!                 ! --   !(WHICH LINE?)    !  STATUS AT USER INTERFACE
  52 FF!                 ! --   !                 !  CONN. J1 AND COMPLEMENT IT.
  53 C7!                 !LDPI  !HL               !Set the pointer to the memory
  54 C3!                 ! --   !2072 hex         !  location of the third port's
  55 72!                 ! --   !                 !  bit status.
  56 20!                 ! --   !                 !
  57 FE!                 !DCR   !B                !Find the correct port routine
  58 CD!                 ! --   !                 !  for the bit (I/O line) to
  59 74!                 !JPRS  !ZERO             !  be complemented.
  5A 20!                 ! --   !THIRD PORT A     !CONN.    PORT *    BIT STATUS
  5B 4B!                 !DCP   !HL               !       PORT 50  1ST   BSA
  5C FE!                 !DCR   !B                ! J1    PORT 51  2ND   BSA+1
  5D CD!                 ! --   !                 !       PORT 52  3RD   BSA+2
  5E 74!                 !JPRS  !ZERO             !       PORT 54  1ST   BSA+3
  5F 11!                 ! --   !SECOND PORT A    ! J2    PORT 55  2ND   BSA+4
1360 4B!                 !DCP   !HL               !       PORT 56  3RD   BSA+5
  61 FE!                 !DCR   !B                !       *=AS SHIPPED
  62 CD!                 ! --   !                 !
  63 74!                 !JPRS  !ZERO             !
  64 02!                 ! --   !FIRST PORT A     !
  65 F9!                 !SEC   !                 !Invalid bit number.  Set carry
  66 C3!                 !RTS   !UN               !  bit to 1 and return.
  67 8A!FIRST PORT A     !LDR   !B,A              !Update port 50 (as shipped)
  68 E8!                 ! --   !                 !  at user interface conn. J1
  69 E4!                 !IPA   !                 !  and update the bit status
  6A 50!                 ! --   !50 hex           !  in memory.
  6B 32!                 !XRA   !B                !
  6C C5!                 ! --   !                 !
  6D E6!                 !OPA   !                 !
  6E 50!                 ! --   !50 hex           !
  6F EB!                 !JPRS  !UN               !
1370 2F!                 ! --   !(UPDATE MEMORY)  !
  71 8A!SECOND PORT A    !LDR   !B,A              !Update port 51 (as shipped)
  72 E8!                 ! --   !                 !  at user interface conn. J1
  73 E4!                 !IPA   !                 !  and update the bit status
  74 51!                 ! --   !51 hex           !  in memory.
  75 32!                 !XRA   !B                !
  76 C5!                 ! --   !                 !
  77 E6!                 !OPA   !                 !
  78 51!                 ! --   !51 hex           !
  79 EB!                 !JPRS  !UN               !
  7A 25!                 ! --   !(UPDATE MEMORY)  !Update port 52 (as shipped)
  7B 8A!THIRD PORT A     !LDR   !B,A              !  at user interface conn. J1
  7C E8!                 ! --   !                 !  and update the bit status
  7D E4!                 !IPA   !                 !  in memory.
  7E 52!                 ! --   !52 hex           !
  7F 32!                 !XRA   !B                1
```

Figure 4-14. (Continued)

```
ADRdata!     LABEL       !INSTR !     MODIFIER     !          COMMENTS
-------!-----------------!------!------------------!-----------------------------
1380 C5!                 ! --   !                  !
  81 E6!                 !OPA   !                  !
  82 52!                 ! --   !52 hex            !
  83 EB!                 !JPRS  !UN                !
  84 1B!                 ! --   !(UPDATE MEMORY)   !
  85 FF!                 !      !                  !
  86 FF!                 !      !                  !
  87 FF!                 !      !                  !
  88 FF!                 !      !                  !
  89 FF!                 !      !                  !
  8A FF!                 !      !                  !
  8B FF!                 !      !                  !
  8C FF!                 !      !                  !
  8D FF!                 !      !                  !
  8E FF!                 !      !                  !
  8F FF!                 !      !                  !
1390 FF!                 !      !                  !
  91 FF!                 !      !                  !
  92 FF!                 !      !                  !
  93 FF!                 !      !                  !
  94 FF!                 !      !                  !
  95 FF!                 !      !                  !
  96 FF!                 !      !                  !
  97 FF!                 !      !                  !
  98 FF!                 !      !                  !
  99 FF!                 !      !                  !
  9A FF!                 !      !                  !
  9B FF!                 !      !                  !
  9C FF!                 !      !                  !
  9D FF!                 !      !                  !
  9E FF!                 !      !                  !
  9F FF!                 !      !                  !
13A0 22!(UPDATE MEMORY)  !ANA   !B                 !Mask all but the changed bit.
  A1 C5!                 ! --   !                  !
  A2 8A!                 !LDR   !C,A               !Save the changed bit in reg C.
  A3 C8!                 ! --   !                  !
  A4 8A!                 !LDA   !B                 !Use reg. B as bit mask.
  A5 C5!                 ! --   !                  !
  A6 F6!                 !CMA   !                  !
  A7 D0!                 ! --   !                  !
  A8 8A!                 !LDR   !B,A               !
  A9 E8!                 ! --   !                  !
  AA 8A!                 !LDAN  !HL                !
  AB 07!                 ! --   !                  !
  AC 22!                 !ANA   !B                 !Mask out the changed bit.
  AD C5!                 ! --   !                  !
  AE 0A!                 !ORA   !C                 !OR in the changed bit.
  AF C1!                 ! --   !                  !
13B0 88!                 !STAN  !(HL)              !Store new bit status in mem.
  81 07!                 ! --   !                  !
  82 C3!                 !RTS   !UN                !RETURN
  83 FF!                 !      !                  !
  84 FF!                 !      !                  !
  85 FF!                 !      !                  !
  86 FF!                 !      !                  !
  87 FF!                 !      !                  !
  88 FF!                 !      !                  !
  89 FF!                 !      !                  !
  8A FF!                 !      !                  !
  8B FF!                 !      !                  !
  8C FF!                 !      !                  !
  8D FF!                 !      !                  !
  8E FF!                 !      !                  !
  8F FF!                 !      !                  !
```

Figure 4-14. (Continued)

```
ADRdata!     LABEL       !INSTR !     MODIFIER    !           COMMENTS
-------!----------------!------!-----------------!-----------------------------
13C0 8A!(SET A BIT)      !LDR   !B,A              !DETERMINE THE OUTPUT MODULE TO
  C1 E8!                 ! --   !                 !  BE TURNED ON (I/O LINE LOW).
  C2 51!                 !PSP   !BC               !  TEST THE BIT THAT CONTROLS
  C3 E8!                 !JSR   !UN               !  THE STATUS OF THE MODULE,
  C4 3A!                 ! --   !(TEST A BIT)     !  AND IF NOT SET, SET IT.
  C5 00!                 ! --   !                 !
  C6 59!                 !PLP   !BC               !
  C7 72!                 !JPRS  !CARRY            !Set C=1 and return if an
  C8 04!                 ! --   !R2               !  invalid bit number.
  C9 8A!                 !LDA   !B                !
  CA C5!                 ! --   !                 !
  CB 74!                 !JPRS  !ZERO             !If the bit is not already set,
  CC 01!                 ! --   !C1               !  complement it and update the
  CD C3!R2               !RTS   !UN               !  bit status in memory.
  CE E8!C1               !JSR   !UN               !
  CF 7F!                 ! --   !(COMPLEMENT BIT)!
13D0 FF!                 ! --   !                 !
  D1 C3!                 !RTS   !UN               !RETURN
  D2 FF!                 !      !                 !
  D3 FF!                 !      !                 !
  D4 FF!                 !      !                 !
  D5 FF!                 !      !                 !
  D6 FF!                 !      !                 !
  D7 FF!                 !      !                 !
  D8 FF!                 !      !                 !
  D9 FF!                 !      !                 !
  DA FF!                 !      !                 !
  DB FF!                 !      !                 !
  DC FF!                 !      !                 !
  DD FF!                 !      !                 !
  DE FF!                 !      !                 !
  DF FF!                 !      !                 !
13E0 8A!(CLEAR A BIT)    !LDR   !B,A              !DETERMINE THE OUTPUT MODULE TO
  E1 E8!                 ! --   !                 !  BE TURNED OFF (I/O LINE HI).
  E2 51!                 !PSP   !BC               !  TEST THE BIT THAT CONTROLS
  E3 E8!                 !JSR   !UN               !  THE STATUS OF THE MODULE,
  E4 1A!                 ! --   !(TEST A BIT)     !  AND IF NOT CLEARED,CLEAR IT.
  E5 00!                 ! --   !                 !
  E6 59!                 !PLP   !BC               !
  E7 72!                 !JPRS  !CARRY            !Set C=1 and return if an
  E8 04!                 ! --   !R3               !  invalid bit number.
  E9 8A!                 !LDA   !B                !
  EA C5!                 ! --   !                 !
  EB 75!                 !JPRS  !NOT ZERO         !If the bit is not already
  EC 01!                 ! --   !C2               !  cleared, complement it and
  ED C3!R3               !RTS   !UN               !  update bit status in memory.
  EE E8!C2               !JSR   !UN               !
  EF 5F!                 ! --   !(COMPLEMENT BIT)!
13F0 FF!                 ! --   !                 !
  F1 C3!                 !RTS   !UN               !RETURN.
  F2 FF!                 !      !                 !
  F3 FF!                 !      !                 !
  F4 FF!                 !      !                 !
  F5 FF!                 !      !                 !
  F6 FF!                 !      !                 !
  F7 FF!                 !      !                 !
  F8 FF!                 !      !                 !
  F9 FF!                 !      !                 !
  FA FF!                 !      !                 !
  FB FF!                 !      !                 !
  FC FF!                 !      !                 !
  FD FF!                 !      !                 !
  FE FF!                 !      !                 !
  FF FF!                 !      !                 !
```

Figure 4-14. (Continued)

```
ADRdata!     LABEL      !INSTR !     MODIFIER    !          COMMENTS
-------!----------------!------!-----------------!----------------------------
1400 E8!(TEST A BIT)    !JSR   !UN               !DETERMINE THE HIGH/LOW STATUS
  01 2D!                ! --   !(WHICH LINE?)    !  OF AN I/O LINE AT THE USER
  02 FF!                ! --   !                 !  INTERFACE CONN.
  03 C7!                !LDPI  !HL               !Set the pointer to the third
  04 C3!                ! --   !2072 hex         !  port's bit status.
  05 72!                ! --   !                 !
  06 20!                ! --   !                 !
  07 FE!                !DCR   !B                !Find the correct port routine
  08 CD!                ! --   !                 !  for the bit to be checked.
  09 74!                !JPRS  !ZERO             !
  0A 18!                ! --   !THIRD PORT B     !
  0B 4B!                !DCP   !HL               !
  0C FE!                !DCR   !B                !
  0D CD!                ! --   !                 !
  0E 74!                !JPRS  !ZERO             !
  0F 0D!                ! --   !SECOND PORT B    !
1410 4B!                !DCP   !HL               !
  11 FE!                !DCR   !B                !
  12 CD!                ! --   !                 !
  13 74!                !JPRS  !ZERO             !
  14 02!                ! --   !FIRST PORT B     !
  15 F9!                !SEC   !                 !Invalid bit number.  Set the
  16 C3!                !RTS   !                 !  carry bit to 1 and return.
  17 8A!FIRST PORT B    !LDR   !B,A              !Save the mask.
  18 E8!                ! --   !                 !
  19 E4!                !IPA   !                 !Input the port (as shipped) at
  1A 50!                ! --   !50 hex           !  the bit to be checked (J1).
  1B EB!                !JPRS  !UN               !Update the bit status in mem.
  1C 0A!                ! --   !UPDATE FLAGS     !
  1D 8A!SECOND PORT B   !LDR   !B,A              !Save the mask.
  1E E8!                ! --   !                 !
  1F E4!                !IPA   !                 !Input the port (as shipped) of
1420 51!                ! --   !51 hex           !  the bit to be checked (J1).
  21 EB!                !JPRS  !UN               !Update the bit status in mem.
  22 04!                ! --   !UPDATE FLAGS     !
  23 8A!THIRD PORT B    !LDR   !B,A              !Save the mask.
  24 E8!                ! --   !                 !
  25 E4!                !IPA   !                 !Input the port (as shipped) of
  26 52!                ! --   !52 hex           !  the bit to be checked (J1).
  27 22!UPDATE FLAGS    !ANA   !B                !SET FLAG STATUS:
  28 C5!                ! --   !                 !  P=0: NO CHANGE
  29 50!                !PSP   !AF               !  P=1: BIT HAS CHANGED SINCE
  2A 9C!                ! --   !                 !       LAST TEST.
  2B 8A!                !LDAN  !(HL)             !  Z=0: BIT IS SET (I/O LINE
  2C 07!                ! --   !                 !       IS LOW).
  2D 22!                !ANA   !B                !  Z=1: BIT IS CLEAR (I/O LINE
  2E C5!                ! --   !                 !       IS HIGH).
  2F 8A!                !LDR   !C,A              !
1430 C8!                ! --   !                 !
  31 9D!                !PLP   !AF               !
  32 58!                ! --   !                 !
  33 90!                !NOP   !                 !
  34 90!                !NOP   !                 !
  35 50!                !PSP   !AF               !
  36 9C!                ! --   !                 !
  37 51!                !PSP   !BC               !Save old data.
  38 E8!                !JSR   !UN               !Update memory to the present
  39 65!                ! --   !(UPDATE MEMORY)  !  bit status.
  3A FF!                ! --   !                 !
  3B 59!                !PLP   !BC               !Put old data back into reg. A
  3C 8A!                !LDA   !C                !
  3D C1!                ! --   !                 !
  3E 59!                !PLP   !BC               !Put new data and flags into BC
  3F 5A!                !PLP   !DE               !
```

Figure 4-14. (Continued)

```
ADRdata!     LABEL       !INSTR !     MODIFIER    !           COMMENTS
-------!----------------!------!-----------------!----------------------------
1440 8A!                 !LDR   !B,E               !
  41 EA!                 ! --   !                 !
  42 32!                 !XRA   !B                !XOR old and new data.ZO=change
  43 C5!                 ! --   !                 !
  44 50!                 !PSP   !AF               !Put "change" flag on stack.
  45 9C!                 ! --   !                 !
  46 8A!                 !LDA   !C                !Put zero flag in reg. A.
  47 C1!                 ! --   !                 !
  48 24!                 !ANAI  !                 !Mask off the sign bit.
  49 7F!                 ! --   !7F hex           !
  4A 59!                 !PLP   !BC               !Pull "change" flag into reg. C
  4B 5A!                 !PLP   !DE               !Position stack pointer.
  4C 90!                 !NOP   !                 !
  4D 90!                 !NOP   !                 !
  4E 8A!                 !LDR   !B,A              !Put the zero flag into reg. B
  4F E8!                 ! --   !                 !
1450 8A!                 !LDA   !C                !Complement "change" flag and
  51 C1!                 ! --   !                 !  rotate into sign position.
  52 F6!                 !CMA   !                 !
  53 DO!                 ! --   !                 !
  54 DO!                 !RLA   !                 !
  55 CO!                 ! --   !                 !
  56 24!                 !ANAI  !                 !
  57 80!                 ! --   !80 hex           !
  58 OA!                 !ORA   !B                !OR "change" and "bit" flags.
  59 C5!                 ! --   !                 !
  5A 8A!                 !LDR   !C,A              !Put the flags into reg. C.
  5B C8!                 ! --   !                 !
  5C 8A!                 !LDR   !E,B              !
  5D D5!                 ! --   !                 !
  5E 52!                 !PSP   !DE               !Set the flag register.
  5F 51!                 !PSP   !BC               !
1460 9D!                 !PLP   !AF               !Set the flag bit.
  61 58!                 ! --   !                 !
  62 C3!                 !RTS   !UN               !Return
  63 FF!                 !      !                 !
  64 FF!                 !      !                 !
  65 FF!                 !      !                 !
  66 FF!                 !      !                 !
  67 FF!                 !      !                 !
  68 FF!                 !      !                 !
  69 FF!                 !      !                 !
  6A FF!                 !      !                 !
  6B FF!                 !      !                 !
  6C FF!                 !      !                 !
  6D FF!                 !      !                 !
  6E FF!                 !      !                 !
  6F FF!                 !      !                 !
1470 50!(TEST INPUT BIT)!PSP   !AF               !CLEAR THE LATCHED BIT OF THE
  71 9C!                 ! --   !                 !  I/O LINE AT THE USER INTER.
  72 E8!                 !JSR   !UN               !  CONN. WHICH IS TO BE USED
  73 BB!                 ! --   !(WHICH LINE?)    !  AS AN INPUT. INPUT THE PORT,
  74 FE!                 ! --   !                 !  AND UPDATE BIT STATUS.
  75 F6!                 !CMA   !                 !
  76 DO!                 ! --   !                 !
  77 FE!                 !DCR   !B                !Find the correct port routine
  78 CD!                 ! --   !                 !  for the bit to be checked.
  79 74!                 !JPRS  !ZERO             !
  7A 20!                 ! --   !THIRD PORT C     !
  7B FE!                 !DCR   !B                !
  7C CD!                 ! --   !                 !
  7D 74!                 !JPRS  !ZERO             !
  7E 12!                 ! --   !SECOND PORT C    !
  7F FE!                 !DCR   !B                !
```

Figure 4-14. (Continued)

```
ADRdata!     LABEL       !INSTR !     MODIFIER    !          COMMENTS
-------!-----------------!------!-----------------!-----------------------------
1480 CD!                 ! --   !                 !
  81 74!                 !JPRS  !ZERO             !
  82 04!                 ! --   !FIRST PORT C     !
  83 9D!                 !PLP   !AF               !
  84 58!                 ! --   !                 !
  85 F9!                 !SEC   !                 !Invalid bit number.  Set carry
  86 C3!                 !RTS   !UN               !  bit to 1 and return.
  87 8A!FIRST PORT C     !LDR   !B,A              !Clear the bit at J1 port 50
  88 E8!                 ! --   !                 !  (as shipped) used as input.
  89 E4!                 !IPA   !                 !
  8A 50!                 ! --   !50 hex           !
  8B 22!                 !ANA   !B                !
  8C C5!                 ! --   !                 !
  8D E6!                 !OPA   !                 !
  8E 50!                 ! --   !50 hex           !
  8F EB!                 !JPRS  !UN               !
1490 12!                 ! --   !PULL             !
  91 8A!SECOND PORT C    !LDR   !B,A              !Clear the bit at J1 port 51
  92 E8!                 ! --   !                 !  (as shipped) used as input.
  93 E4!                 !IPA   !                 !
  94 51!                 ! --   !51 hex           !
  95 22!                 !ANA   !B                !
  96 C5!                 ! --   !                 !
  97 E6!                 !OPA   !                 !
  98 51!                 ! --   !51 hex           !
  99 EB!                 !JPRS  !UN               !
  9A 08!                 ! --   !PULL             !
  9B 8A!THIRD PORT C     !LDR   !B,A              !Clear the bit at J1 port 52
  9C E8!                 ! --   !                 !  (as shipped) used as input.
  9D E4!                 !IPA   !                 !
  9E 52!                 ! --   !52 hex           !
  9F 22!                 !ANA   !B                !
14A0 C5!                 ! --   !                 !
  A1 E6!                 !OPA   !                 !
  A2 52!                 ! --   !52 hex           !
  A3 9D!PULL             !PLP   !AF               !Restore registers.
  A4 58!                 ! --   !                 !
  A5 E9!                 !JPR   !UN               !Check the status of the input
  A6 58!                 ! --   !(TEST A BIT)     !  module and update bit status
  A7 FF!                 ! --   !                 !
  A8 FF!                 !      !                 !
  A9 FF!                 !      !                 !
  AA FF!                 !      !                 !
  AB FF!                 !      !                 !
  AC FF!                 !      !                 !
  AD FF!                 !      !                 !
  AE FF!                 !      !                 !
  AF FF!                 !      !                 !
14B0 B0!(PWR ON)         !LDAI  !                 !TURN ON MODULE RACK POWER
  B1 00!                 ! --   !00 hex           !  +VCC A.
  B2 E6!                 !OPA   !                 !
  B3 53!                 ! --   !53 hex           !
  B4 C3!                 !RTS   !UN               !RETURN
  B5 FF!                 !      !                 !
  B6 FF!                 !      !                 !
  B7 FF!                 !      !                 !
14B8 B0!(PWR OFF)        !LDAI  !                 !TURN OFF MODULE RACK POWER
  B9 80!                 ! --   !80 hex           !  +VCC A.
  BA E6!                 !OPA   !                 !
  BB 53!                 ! --   !53 hex           !
  BC C3!                 !RTS   !UN               !RETURN
  BD FF!                 !      !                 !
  BE FF!                 !      !                 !
  BF FF!                 !      !                 !
```

Figure 4-14. (Continued)

REFERENCE DRAWINGS

The schematic (figure 5-1) and assembly drawing (figure 5-2) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

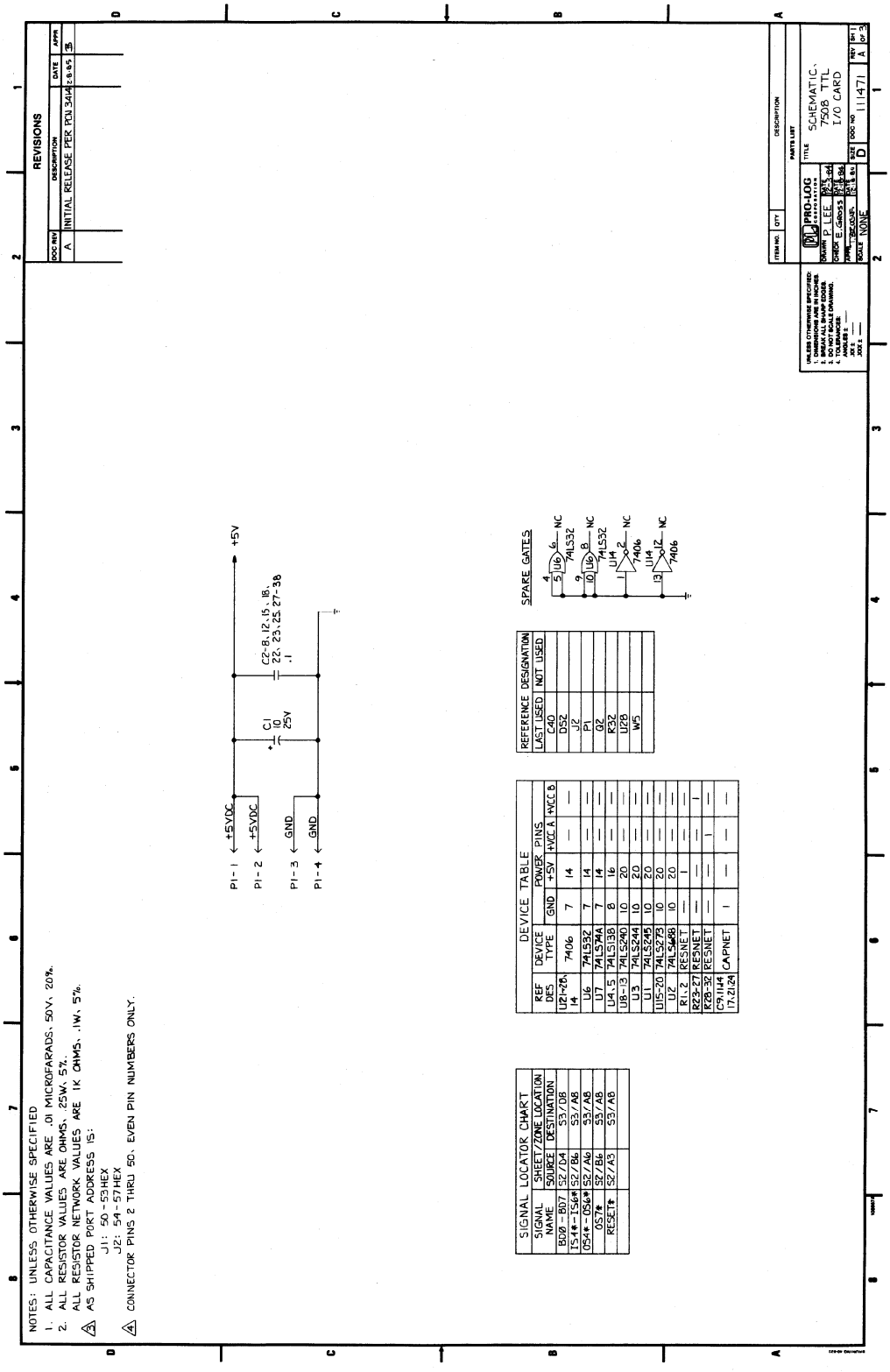

Figure 5-1. Schematic (1 of 3)

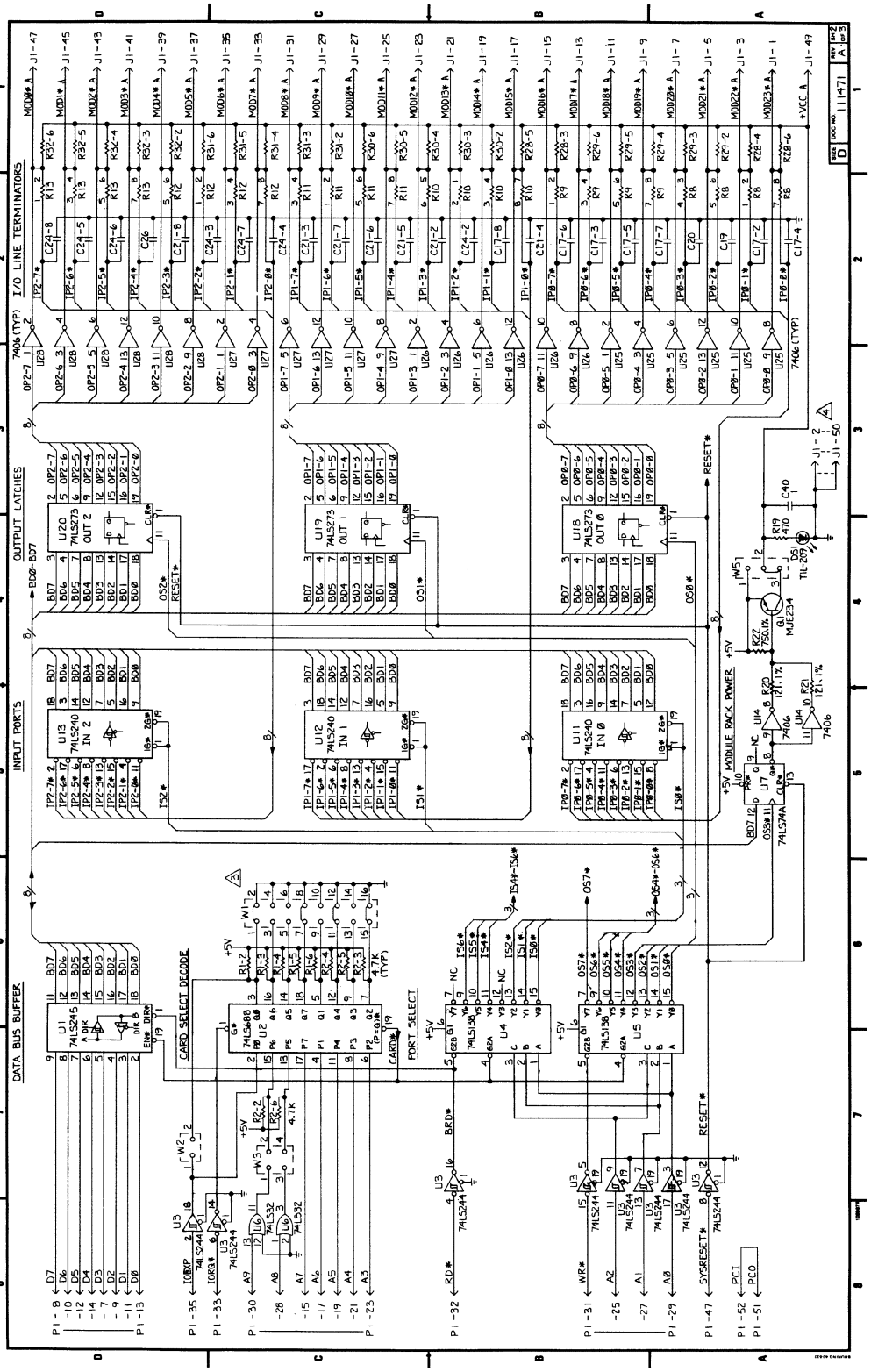

Figure 5-1. Schematic (2 of 3)

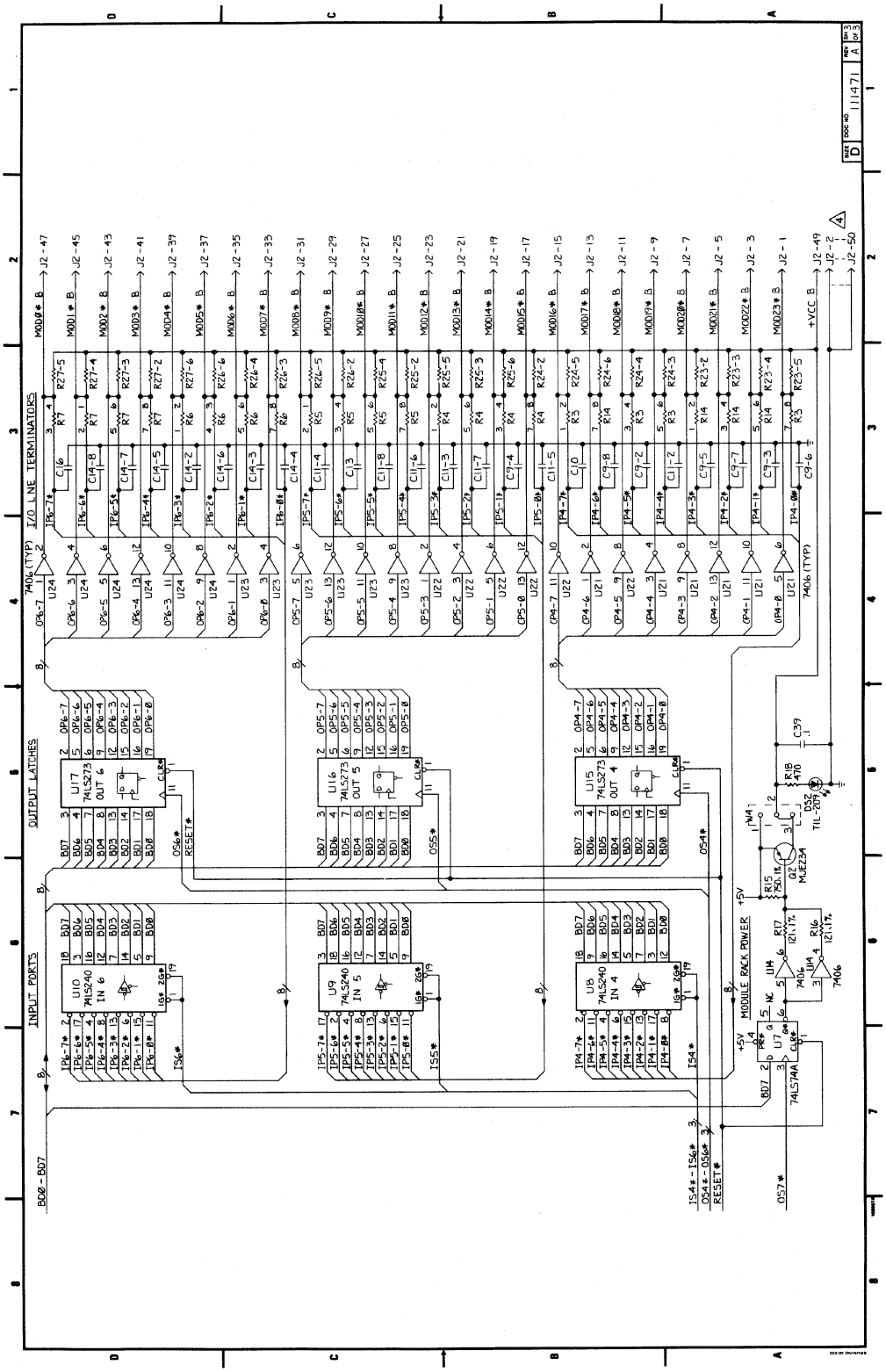

Figure 5-1. Schematic (3 of 3)

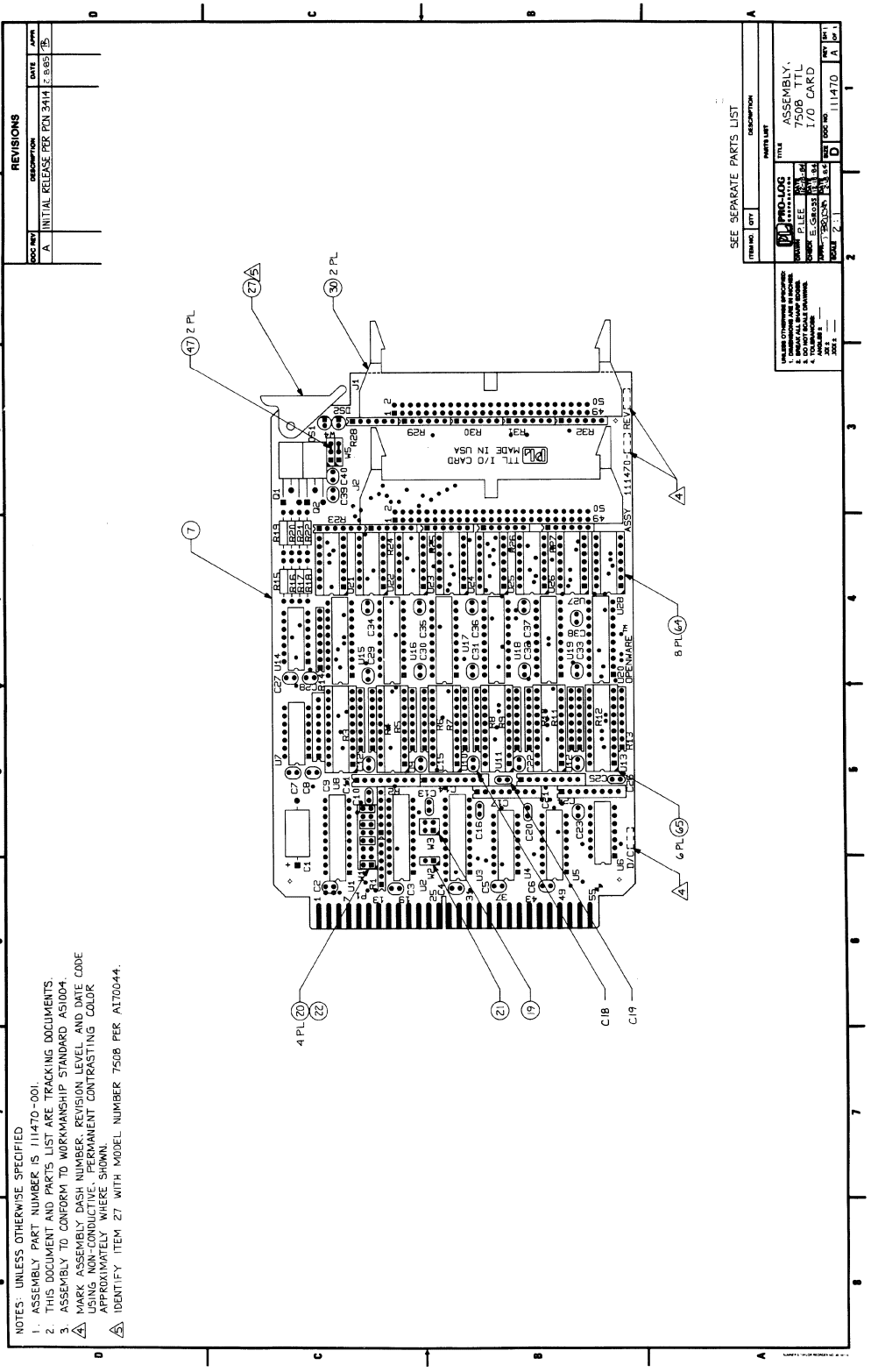
REVISIONS
DESCRIPTION
INITIAL RELEASE PER PCN 3414
SEE SEPARATE PARTS LIST
ASSEMBLY: 7508 TTL I/O CARD
111470
NOTES: UNLESS OTHERWISE SPECIFIED
1. ASSEMBLY PART NUMBER IS 111470-001.
2. THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS.
3. ASSEMBLY TO CONFORM TO WORKMANSHIP STANDARD AS1004.
4. MARK ASSEMBLY DASH NUMBER, REVISION LEVEL AND DATE CODE USING NON-CONDUCTIVE, PERMANENT CONTRASTING COLOR APPROXIMATELY WHERE SHOWN.
5. IDENTIFY ITEM 27 WITH MODEL NUMBER 7508 PER A170044.

Figure 5-2. Assembly Drawing

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   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, and reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

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